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Attorneys for Plaintiff
LONGITUDE LICENSING LIMITED

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

LONGITUDE LICENSING LIMITED,

Plaintiff,

v.

AMAZON.COM, INC.,

Defendant.

Case No

COMPLAINT FOR PATENT INFRINGEMENT

JURY TRIAL DEMANDED

1. Plaintiff Longitude Licensing Limited ("Longitude" or "Plaintiff") for its Complaint against Defendant Amazon.com, Inc. ("Amazon.com" or "Defendant") hereby alleges as follows:

PARTIES

2. Longitude is an entity formed under the laws of Ireland with its principal place of business at Plaza 255 Suite 2A, Blanchardstown Corporate Park 2, Dublin D15 YH6H, Ireland.

3. On information and belief, Defendant Amazon.com, Inc. is a Delaware corporation with its principal place of business at 410 Terry Avenue North, Seattle, Washington 98109.

NATURE OF THE ACTION

4. This is a civil action for the infringement of United States Patent Nos. 7,697,369 (the "'369 patent"), 9,379,233 (the "'233 patent"), RE43,539 the ("'539 Patent"), and 9,207,701 (the "'701 patent") (collectively, the "Patents-in-Suit") under the patent laws of the United States, 35 U.S.C. § 1, et seq.

5. This action involves Defendant's manufacture, use, sale, offer for sale, and/or importation into the United States of infringing products, methods, processes, services and systems that incorporate certain memory chips and components that infringe one or more of the claims of the Patents-in-Suit.

JURISDICTION AND VENUE

6. This Court has original jurisdiction over the subject matter of this Complaint under 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, including 35 U.S.C. §§ 271, et seq.

7. Defendant is subject to personal jurisdiction in this judicial district because Defendant regularly transacts business in this judicial district by, among other things, offering Defendant's products and services to customers, business affiliates and partners located in this judicial district. In addition, Defendant has committed

acts of direct infringement of one or more of the claims of one or more of the Patents-in-Suit in this judicial district.

8. Venue in this district is proper under 28 U.S.C. §§ 1400(b) and 1391(b) and (c), because Defendant is subject to personal jurisdiction in this district and has committed acts of infringement in this district. Longitude is informed and believes that Defendant has regular and established places of business in this District at (1) 923 Westwood Boulevard, Los Angeles, California 90024; (2) 1620 26th Street, Santa Monica, California 90404; and (3) 40 Pacifica Avenue, Irvine, California 92618, among others.

FACTUAL BACKGROUND

9. Longitude operates in one of the most dynamic segments of the international knowledge-based economy. Longitude operates by partnering with patent owners to prosecute and license patent portfolios. The company has also formed customized arrangements that combine exclusive licensing rights and ownership positions, and it also has acquired patents outright from other global patent owners. Longitude has the licensing rights to portfolios totaling nearly 4,000 semiconductor and computer memory patents and patent applications originally filed by well-known technology companies.

10. Longitude is the owner by assignment of the patents-in-suit.

11. Longitude has licensed the patents-in-suit to a majority of the worldwide memory industry responsible for solid state memory devices used in products sold in the United States, including SK Hynix, Kingston, Winbond, Micron, Samsung Electronics and Kioxia (formerly the memory division of Toshiba).

12. One major player in the industry that has refused to license the Patent-in-Suit is Western Digital Corporation ("Western Digital"). Western Digital is a computer hard disk drive manufacturer and data storage company. Western Digital designs, manufactures, and sells data technology products, including storage devices, data

center systems, and cloud storage services. Longitude is informed and believes that Western Digital acquired SanDisk in 2016.

13. Since February 2018, Longitude has requested that Western Digital negotiate licenses for patents (including the Patents-in-Suit) that it is infringing, but Western Digital has refused to negotiate, claiming that Longitude may not assert its licensing rights as a result of covenants in two contracts between Western Digital and third parties that have never owned any of the patents-in-suit. Those contracts do not apply to Longitude, but Western Digital nonetheless contended that it could only be sued after every other market participant (apparently including Western Digital's customers) was sued.

14. Longitude initiated an arbitration claim against Western Digital for declaratory relief concerning Western Digital's interpretation of the agreements. Western Digital objected to the jurisdiction of the arbitration tribunal to avoid any consideration of the merits of contract arguments.

15. After the arbitration against Western Digital was dismissed on jurisdictional grounds, Longitude gave notice to Defendant that it was infringing the patents-in-suit by letter dated September 6, 2022. This letter included a table that identified a number of products that were believed to infringe the patents. Among other things, the letter stated:

> A number of Amazon products incorporate and use features and functionality covered by Longitude patents, including, for example, the patents and exemplary products identified in the attached table ("Table 1"). In reviewing the Table, you will note that the infringing products contain devices manufactured by Western Digital Corporation ("Western Digital"). While our normal approach is to engage with, and license, suppliers such as Western Digital rather than their customers, Western Digital has refused to engage in any licensing discussions. Consequently, we are contacting Western Digital customers who are selling products that infringe Longitude patents.

16. Defendant did not take a license following receipt of this letter and continued to infringe as stated in the letter. As of the filing of this Complaint, Defendant has not responded in any manner to Longitude.

17. Among the other products referenced in the letter was Amazon Echo Show 10, Fire Stick Lite, and all other Amazon products having Western Digital FKB7 NAND flash memory and certain Western Digital NAND memory chips.

THE PATENTS-IN-SUIT

18. Longitude is the owner by assignment of the Patents-in-Suit. Longitude owns all rights to the Patents-in-Suit, including the right to enforce the Patents-in-Suit.

19. All maintenance fees for the Patents-in-Suit have been timely paid, and there are no fees currently due.

20. United States Patent No. 7,697,369, entitled "System with Controller and Memory," issued on April 13, 2010 from United States Patent Application No. 11/759,862 filed on June 7, 2007.

21. United States Patent No. RE43,539, entitled "Output Buffer Circuit and Integrated Semiconductor Circuit Device With Such Output Buffer Circuit," issued on July 24, 2012 from United States Patent Application No. 11/798,773 filed on May 16, 2007. The '539 Patent is a re-issue of U.S. Patent No. 6,894,547, which issued on May 17, 2005 from United States Patent Application No. 10/320,059 filed December 16, 2002.

22. United States Patent No. 9,379,233, entitled "Semiconductor Device," issued on June 28, 2016 from United States Patent Application No. 14/872,844 filed October 1, 2015.

23. United States Patent No. 9,207,701, entitled "Supply Voltage Generating Circuit," issued on December 8, 2015 from United States Patent Application No. 14/480,768 filed on September 9, 2014.

COUNT I

(DEFENDANT'S INFRINGEMENT OF THE '369 PATENT)

24. Paragraphs 1 through 23 are incorporated by reference as if fully restated herein.

25. United States Patent No. 7,697,369, entitled "System with Controller and Memory," issued on April 13, 2010 from United States Patent Application No. 11/759,862 filed on June 7, 2007.

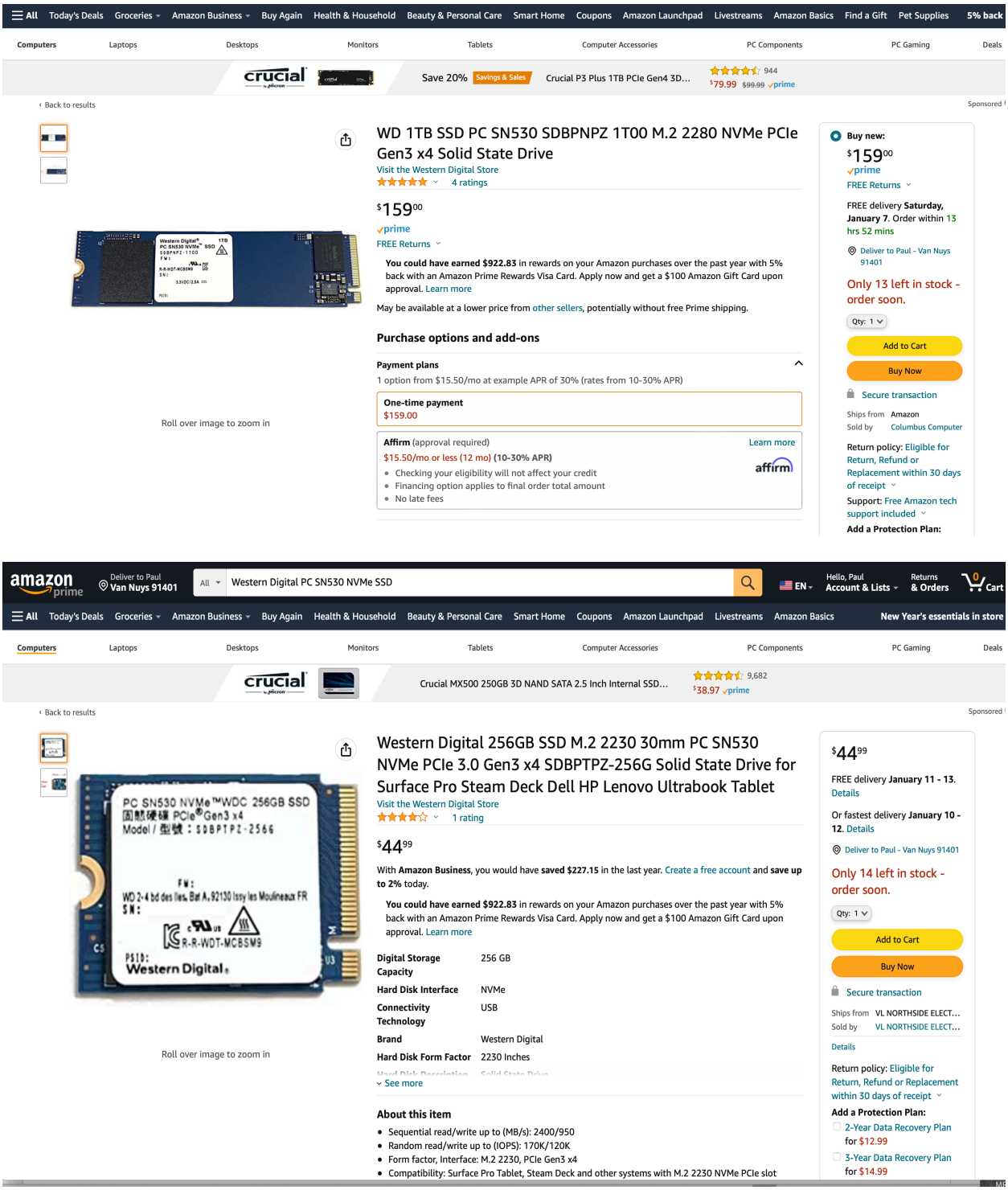
26. Longitude is the owner of the ’369 patent with full rights to pursue recovery of royalties for damages for infringement, including full rights to recover past and future damages.

27. Each claim of the ’369 patent is valid, enforceable, and patent-eligible.

28. Longitude and its predecessors in interest have satisfied the requirements of 35 U.S.C. § 287(a) with respect to the ’369 patent, and Longitude is entitled to damages for Defendant’s past infringement. Among other things, Longitude provided actual notice of infringement to the component supplier, Western Digital.

29. Defendant has directly infringed (literally and equivalently) and induced others to infringe the ’369 patent by making, using, selling, offering for sale, or importing products that infringe the claims of the ’369 patent and by inducing others to infringe the claims of the ’369 patent without a license or permission from Longitude. These products include without limitation Western Digital PC SN530 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the ‘369 patent.

30. A non-limiting example of Defendant’s infringement is its sales and offers for sale of Western Digital PC SN530 NVMe SSDs as demonstrated below.



Western Digital PC SN530 NVMe SSDs infringe at least claim 1 of the '369 patent.

31. Longitude is informed and believes that the Western Digital PC SN530 NVMe SSD Operates in Compliance with the Open NAND Flash Interface Specification, Revision 4.0 dated April 2, 2014 (ONFI Standard).

32. The Western Digital PC SN530 NVMe SSD is a system:

33. The Western Digital PC SN530 NVMe SSD includes a controller:

34. The Western Digital PC SN530 NVMe SSD includes a controller that is adapted to send out a first strobe signal and a write data signal in a write operation, the write data signal being synchronized with the first data strobe signal:

Signal Name	Input / Output	Description
ALE_x	I	**Address Latch Enable** The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). Refer to section 4.3.
WE_x_n	I	**Write Enable** The Write Enable signal controls the latching of commands, addresses, and input data in the SDR data interface. The Write Enable signal controls the latching of commands and addresses in the NV-DDR2 or NV-DDR3 data interface. Data, commands, and addresses are latched on the rising edge of WE_x_n. This signal shares the same pin as CLK_x in the NV-DDR data interface.
CLK_x	I	**Clock** The Clock signal is used as the clock in the NV-DDR data interface. This signal shares the same pin as WE_x_n in the SDR, NV-DDR2, and NV-DDR3 data interface.
WP_x_n	I	**Write Protect** The Write Protect signal disables Flash array program and erase operations. See section 2.19 for requirements.
IO0_0 – IO7_0 (DQ0_0 – DQ7_0)	I/O	**I/O Port 0, bits 0-7** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. Also known as DQ0_0 – DQ7_0 for the NV-DDR, NV-DDR2, and NV-DDR3 data interfaces.
DQS (DQS_x_t)	I/O	**Data Strobe (True)** The data strobe signal that indicates the data valid window for the NV-DDR and NV-DDR2 data interfaces.
DQS_x_c	I/O	**Data Strobe Complement** The Data Strobe Complement signal is the complementary signal to Data Strobe True, optionally used in the NV-DDR2 or NV-DDR3 data interface. Specifically, Data Strobe Complement has the opposite value of Data Strobe True when CE_n is low, i.e. if DQS_x_t is high then DQS_x_c is low; if DQS_x_t is low then DQS_x_c is high.
IO8 – IO15	I/O	**I/O Port 0, bits 8-15** These signals are used in a 16-bit wide target configuration. The signals are the upper 8 bits for the 16-bit wide bidirectional port used to transfer data to and from the device. These signals are only used in the SDR data interface.

and a write data signal **[D]**

adapted to send out a first data strobe signal **[C]**

ONFI Standard at 30.

adapted to send out a first data strobe signal **[C]**

and a write data signal **[D]**

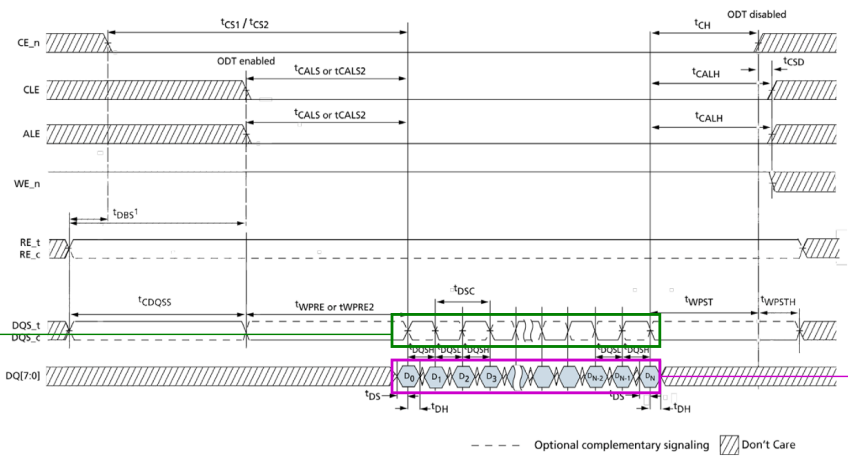
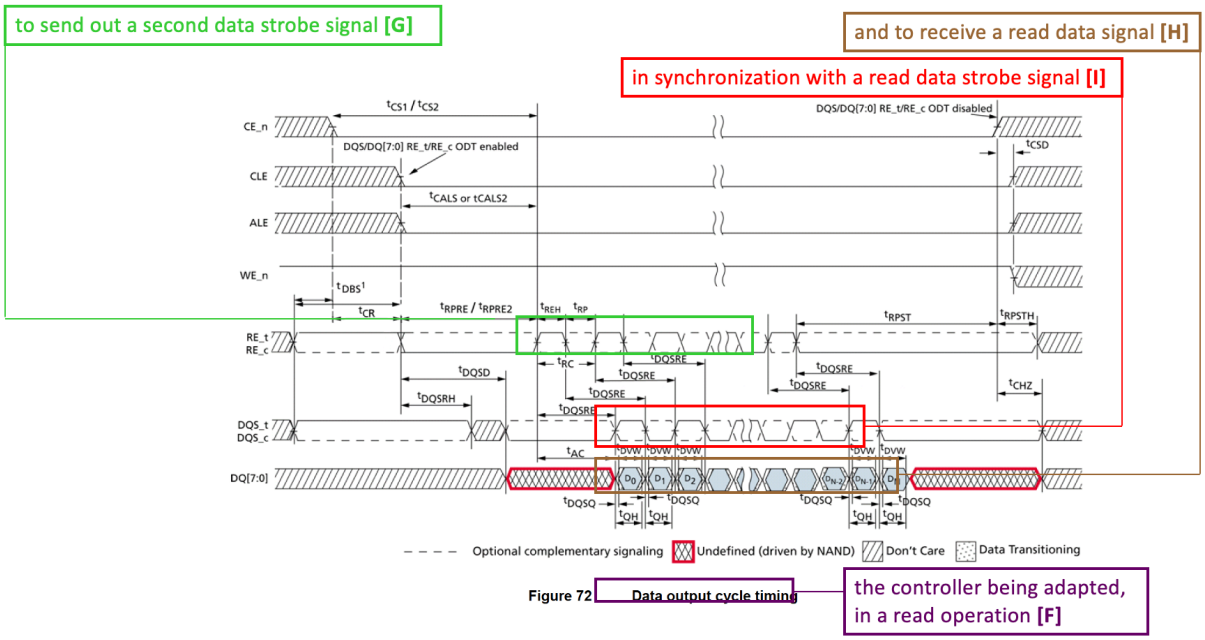


Figure 71 Data input cycle timing

in a write operation, the write data signal being synchronized with the first data strobe signal **[E]**

ONFI Standard at 165.

35. The Western Digital PC SN530 NVMe SSD further includes a controller being adapted in a read operation to send out a second data strobe signal and to receive a read data signal in synchronization with a read strobe signal.



ONFI Standard at 167.

36. The Western Digital PC SN530 NVMe SSD further includes the read strobe signal being received by the controller in response to the second data strobe signal:

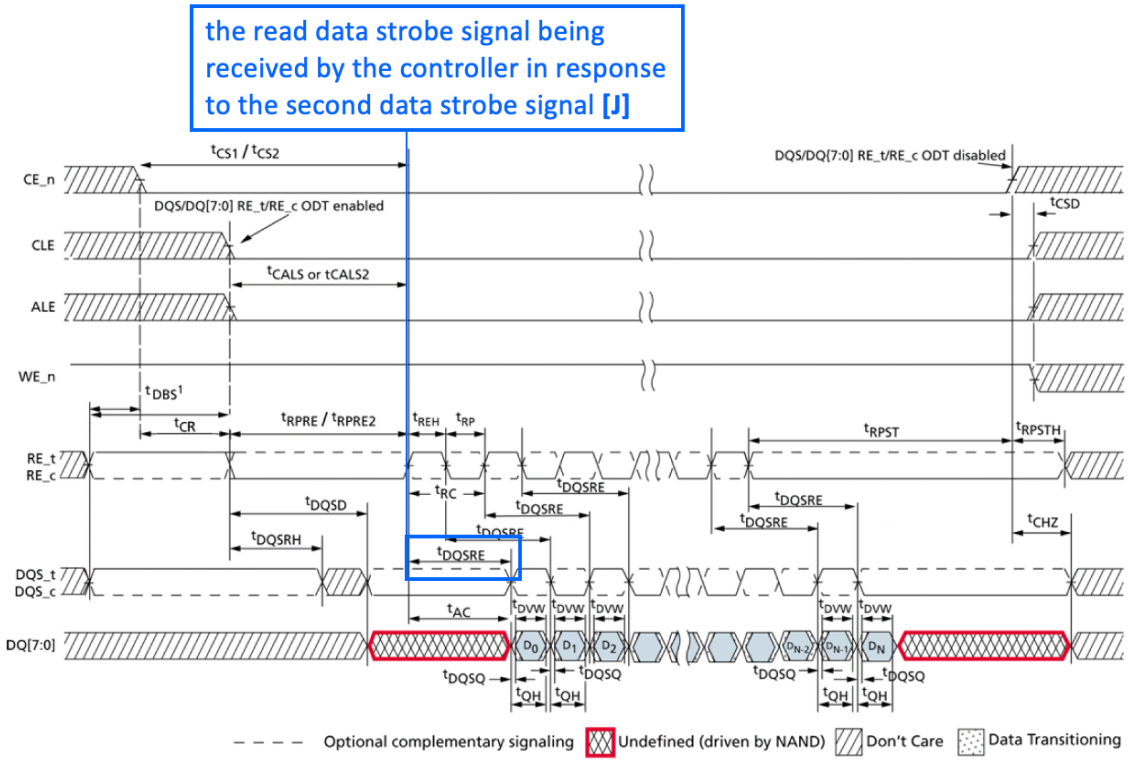
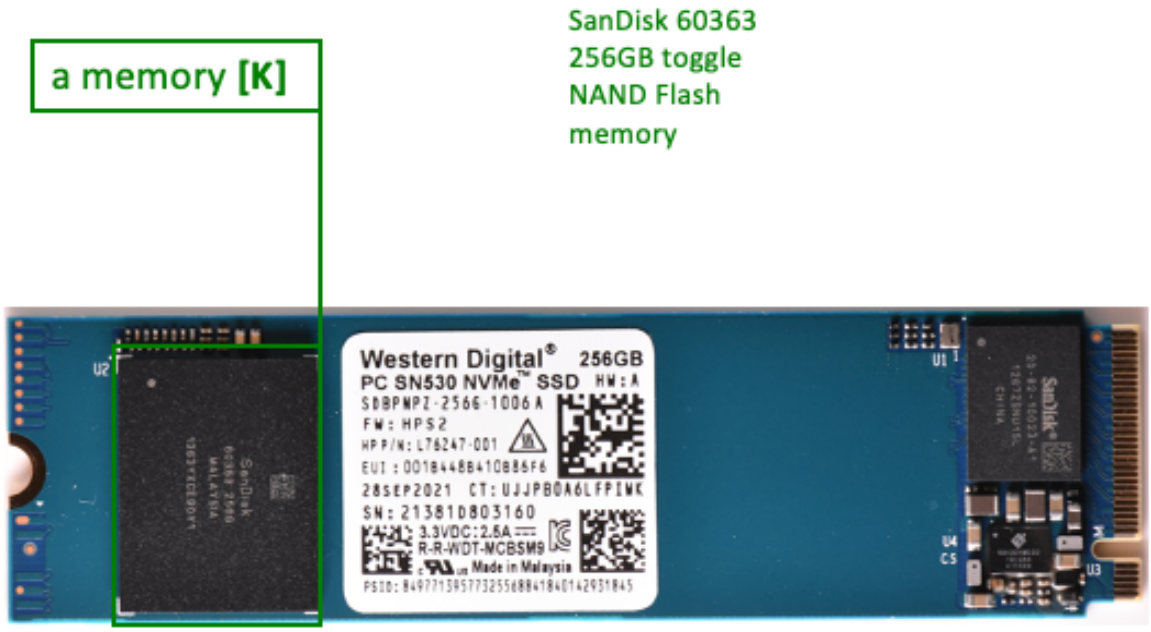


Figure 72 Data output cycle timing

ONFI Standard at 167.

37. The Western Digital PC SN530 NVMe SSD further includes a memory:



38. The Western Digital PC SN530 NVMe SSD further includes a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation:

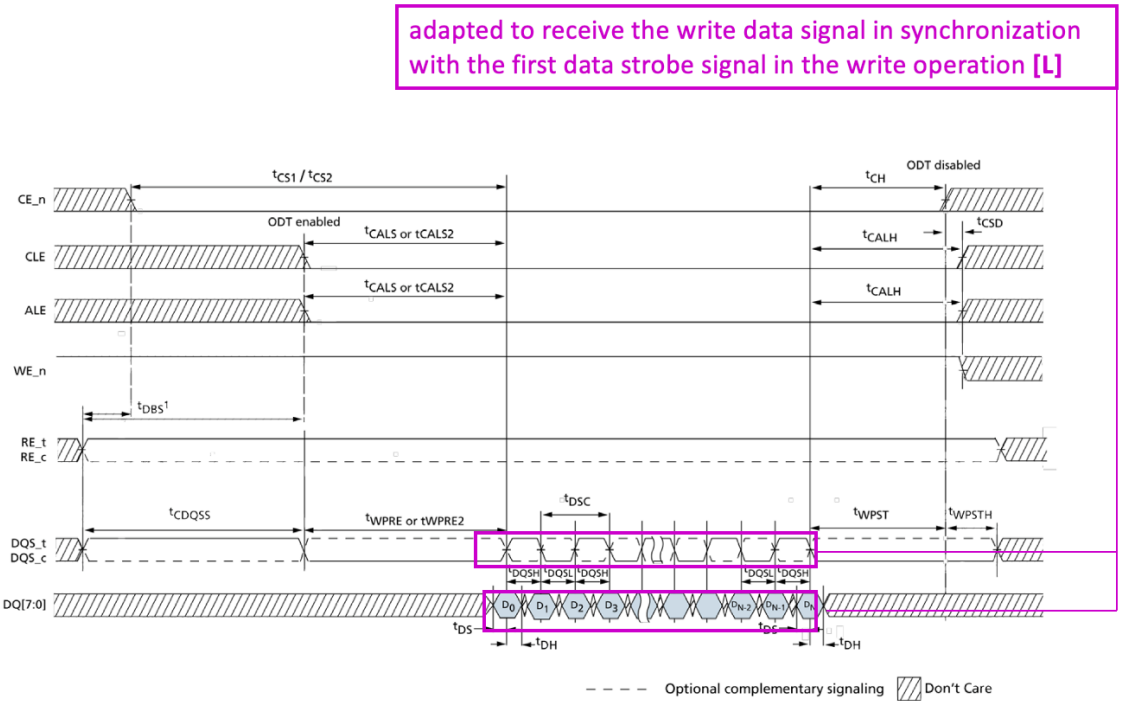


Figure 71 Data input cycle timing

39. The Western Digital PC SN530 NVMe SSD further includes a memory adapted, in the read operation, to output the read data strobe signal in response to the second data strobe signal and to send the read data signal synchronized with the read data strobe signal:

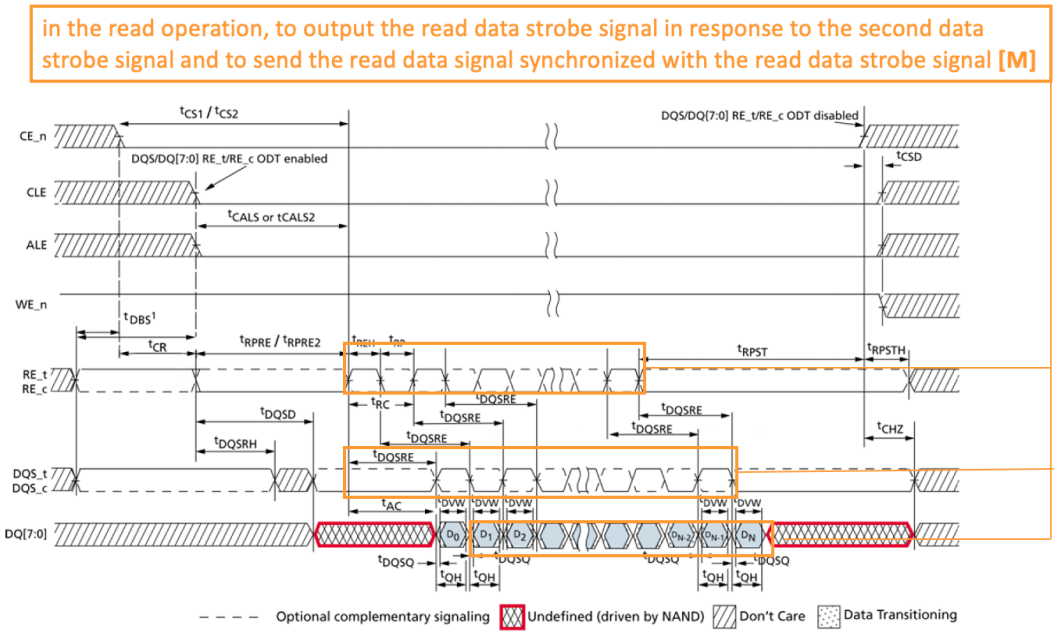


Figure 72 Data output cycle timing

40. Defendant actively, knowingly, and intentionally induces, and continues to actively, knowingly, and intentionally induce, infringement of the '369 patent under 35 U.S.C. §271(b) by its customers and end users.

41. Defendant has had knowledge of and notice of the '369 patent and its infringement since at least September 6, 2022 when Longitude gave Defendant notice of its infringing actions. In any event, Defendant has had knowledge and notice of the '369 patent since at least the filing of this complaint.

42. Defendant has induced its customers and end users to infringe the '369 patent by using its products as shown above. For example, Defendant encourages its customers and end users to perform infringing methods by the very nature of the products.

43. Defendant specifically intends its customers and/or end users infringe the '369 patent, either literally or by the doctrine of equivalents, because Defendant has known about the '369 patent and how Defendant's products infringe the claims of the '369 patent but Defendant has not taken steps to prevent infringement by its customers and/or end users. Accordingly, Defendant has acted with the specific intent to induce infringement of the '369 patent.

44. Accordingly, Defendant has induced, and continues to induce, infringement of the '369 patent under 35 U.S.C. §271(b).

45. As discussed above, Defendant has had knowledge of and notice of the '369 patent and its infringement since at least September 6, 2022. Despite this knowledge, Defendant continues to commit tortious conduct by way of patent infringement.

46. Defendant has been and continues to infringe one or more of the claims of the '369 patent through the aforesaid acts.

47. Defendant has committed these acts of infringement without license or authorization.

48. Plaintiff is entitled to recover damages adequate to compensate for the infringement.

49. Defendant has and continues to infringe the '369 patent, acting with an objectively high likelihood that its actions constitute infringement of the '369 patent. Defendant has known or should have known of this risk at least as early as September 6, 2022. Accordingly, Defendant's infringement of the '369 patent has been and continues to be willful.

COUNT II

(DEFENDANT'S INFRINGEMENT OF THE '539 PATENT)

50. Paragraphs 1 through 49 are incorporated by reference as if fully restated herein.

51. United States Patent No. RE43,539, entitled "Output Buffer Circuit and Integrated Semiconductor Circuit Device With Such Output Buffer Circuit," issued on July 24, 2012 from United States Patent Application No. 11/798,773 filed on May 16, 2007. The '539 Patent is a re-issue of U.S. Patent No. 6,894,547, which issued on May 17, 2005 from United States Patent Application No. 10/320,059 filed December 16, 2002.

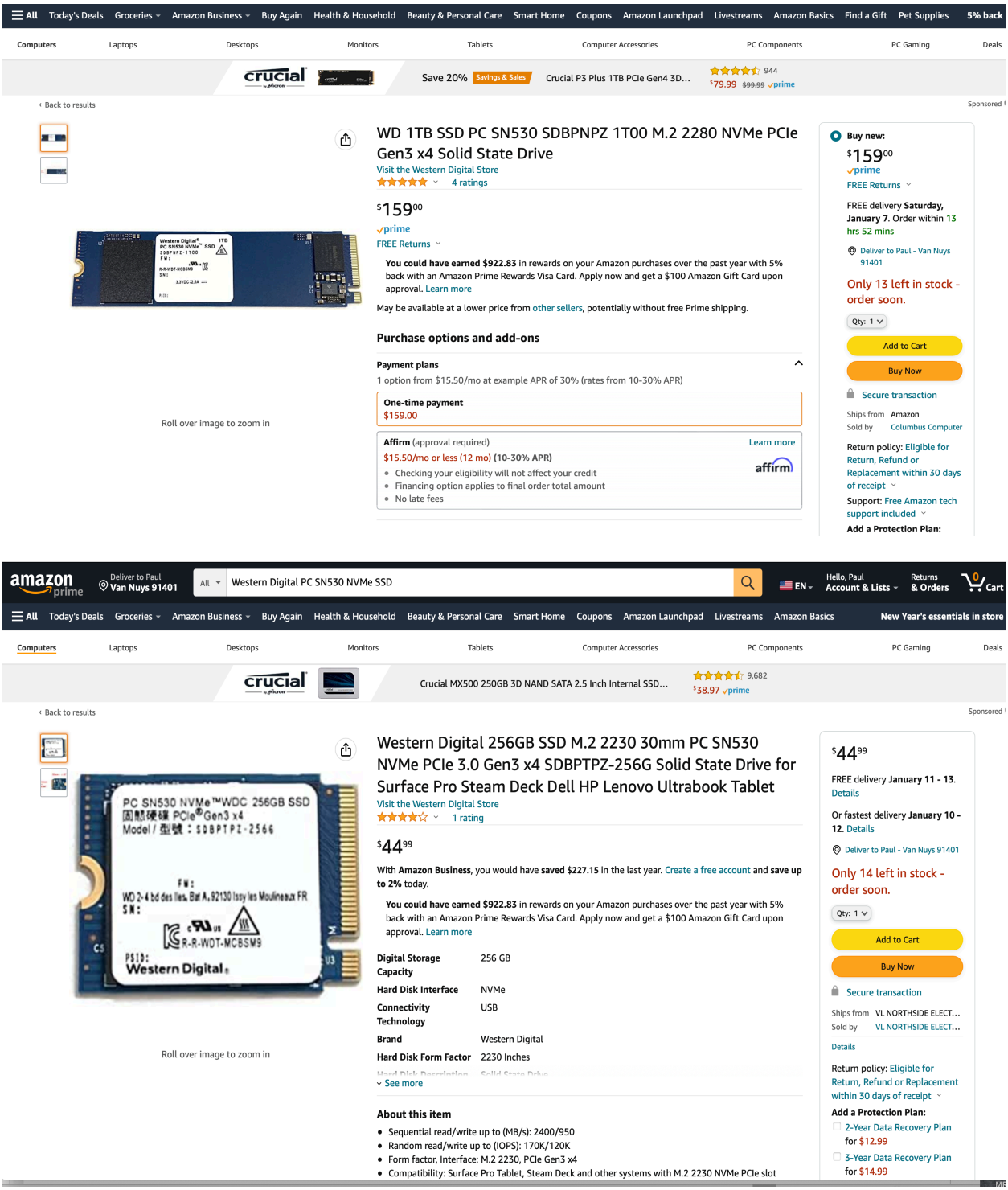
52. Longitude is the owner of the '539 patent with full rights to pursue recovery of royalties for damages for infringement, including full rights to recover past and future damages.

53. Each claim of the '539 patent is valid, enforceable, and patent-eligible.

54. Longitude and its predecessors in interest have satisfied the requirements of 35 U.S.C. § 287(a) with respect to the '539 patent, and Longitude is entitled to damages for Defendant's past infringement. Among other things, Longitude provided actual notice of infringement to the component supplier, Western Digital.

55. Defendant has directly infringed (literally and equivalently) and induced others to infringe the '539 patent by making, using, selling, offering for sale, or importing products that infringe the claims of the '539 patent and by inducing others to infringe the claims of the '539 patent without a license or permission from Longitude. These products include without limitation Western Digital PC SN530 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the '539 patent.

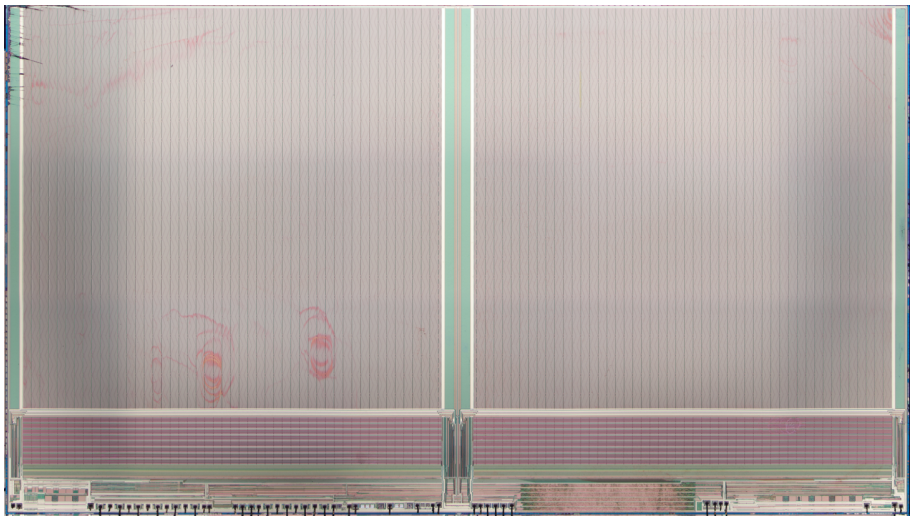
56. A non-limiting example of Defendant's infringement is its sales and offers for sale of Western Digital PC SN530 NVMe SSDs as demonstrated below.



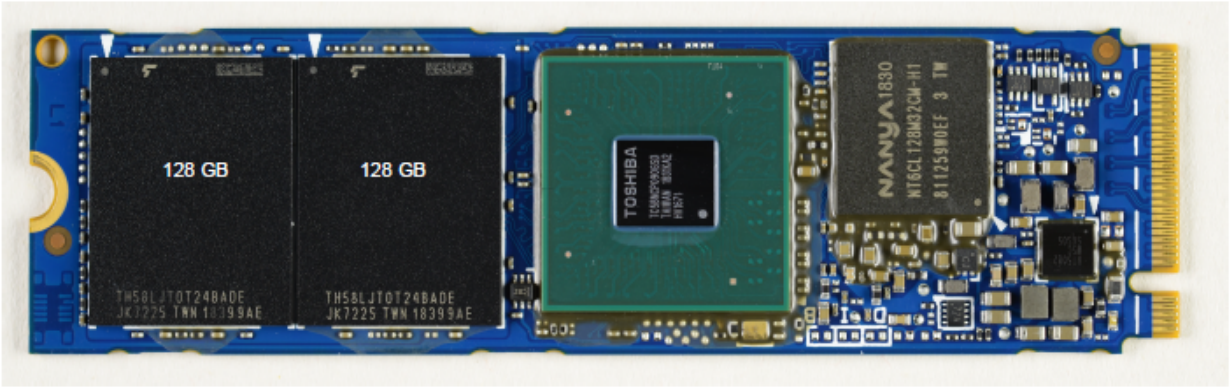
Western Digital PC SN530 NVMe SSDs infringe at least claim 1 of the '539 patent.

57. The Western Digital PC SN530 NVMe SSD includes a SanDisk memory chip:

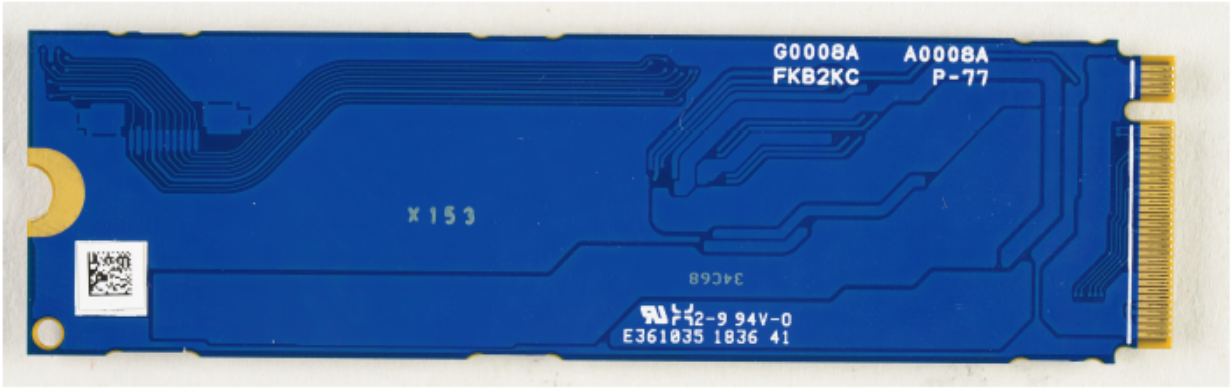
58. The below image shows the pin layout and corners of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD:



59. On information and belief, the Western Digital PC SN530 NVMe SSD is substantially similar to the Toshiba KXG60ZNV256G SSD Package ("Toshiba SSD") for all matters relevant to this complaint. The Toshiba SSD is depicted below:

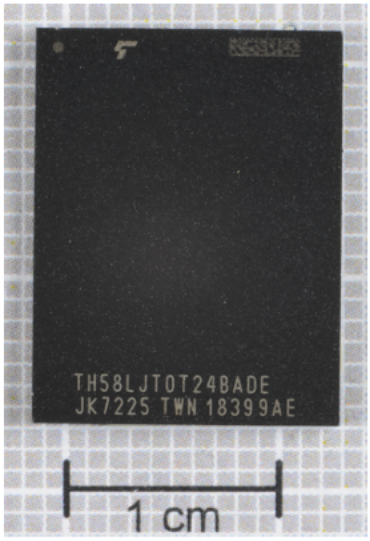


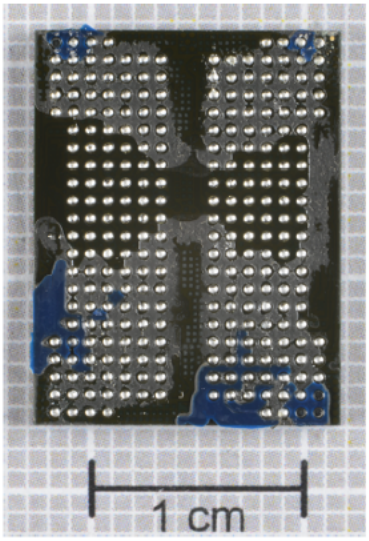
Toshiba KXG60ZNV256G SSD Package – Top

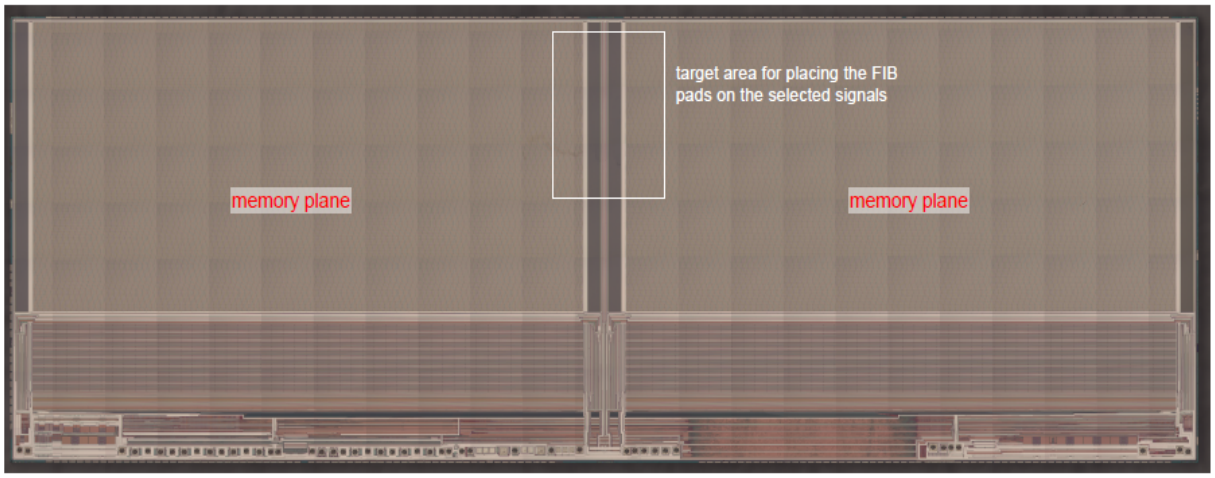


Toshiba KXG60ZNV256G SSD Package – Bottom

60. The memory chip of the Toshiba SSD, the Toshiba TH58LJT0T24BADE Package is depicted in the images below:

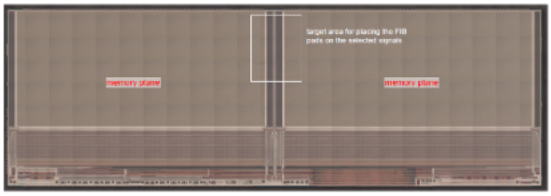




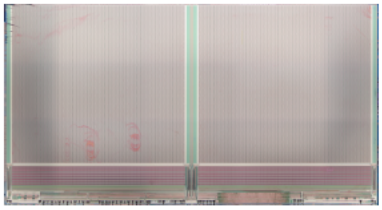


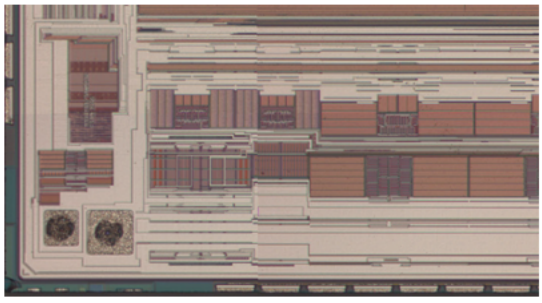
Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

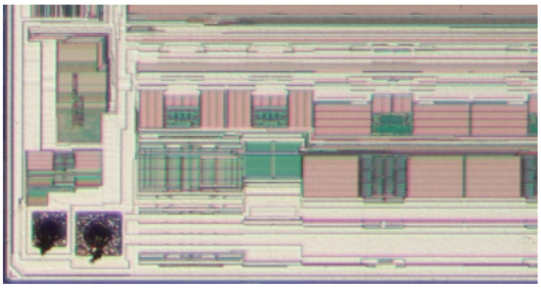
61. A side-by-side comparison of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package used in the Toshiba SSD is depicted below:



Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph



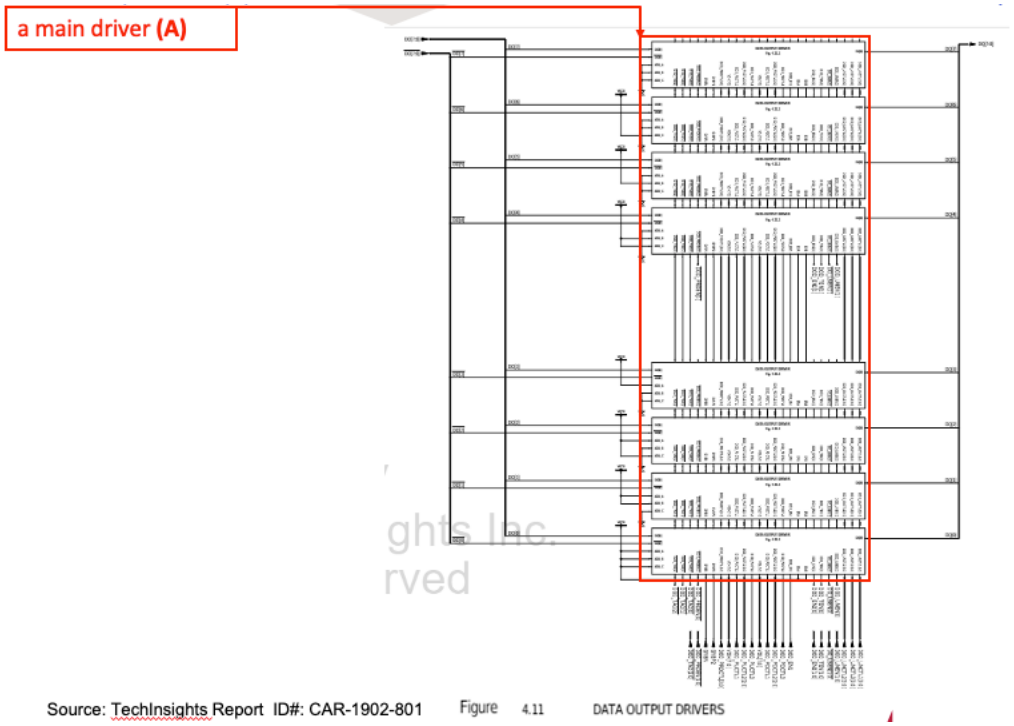




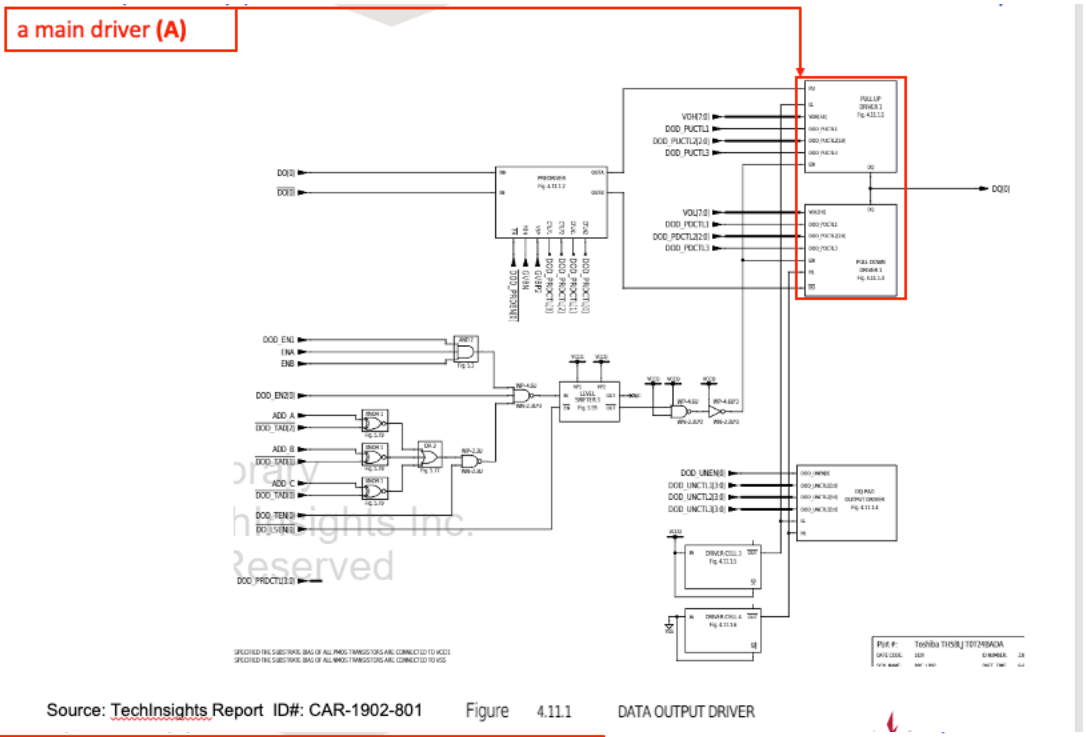
62. Based at least on the above, Longitude is informed and believes, that the corners of the dies of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package are substantially the same. Among other things, the corners are substantially the same. Accordingly, Longitude is informed and believes that the various I/Os and peripheral circuits are the same between the Toshiba and Western Digital/SanDisk chips. Furthermore,

Longitude is informed and believes that Toshiba and Western Digital shared the designs for 96 layer chips. Accordingly, the SanDisk memory chip is substantially the same as the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package. For this reason, Longitude is informed and believes that technical documents and other analysis concerning the Toshiba TH58LJT0T24BADE Package also describe the layout and functionality of the Western Digital PC SN530 NVMe SSD.

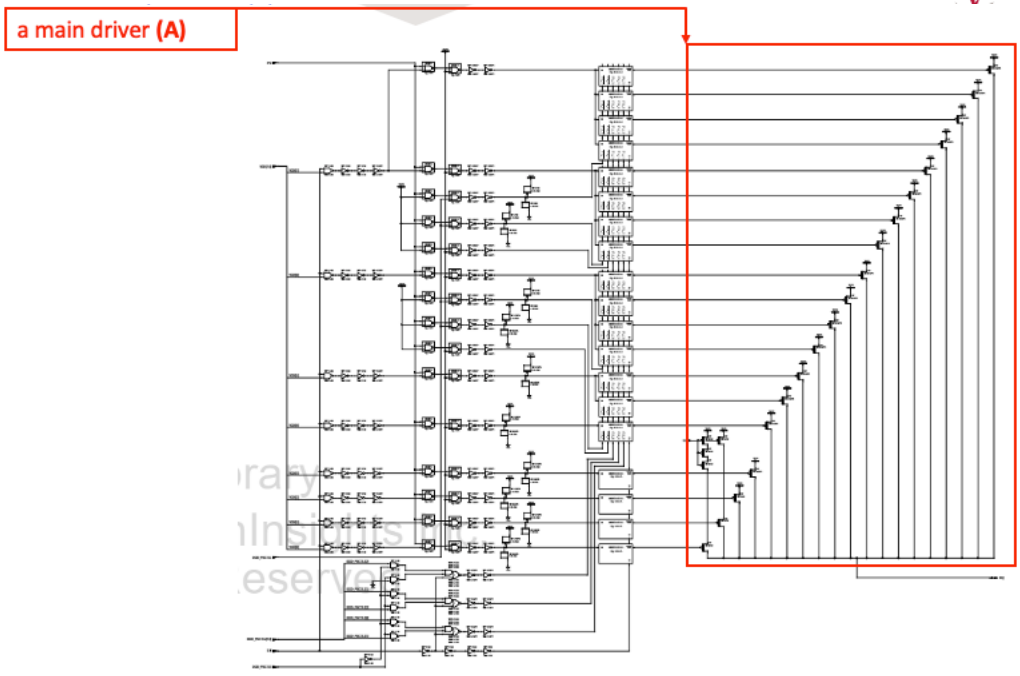
63. The Western Digital PC SN530 NVMe SSD includes an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate comprising a main driver:



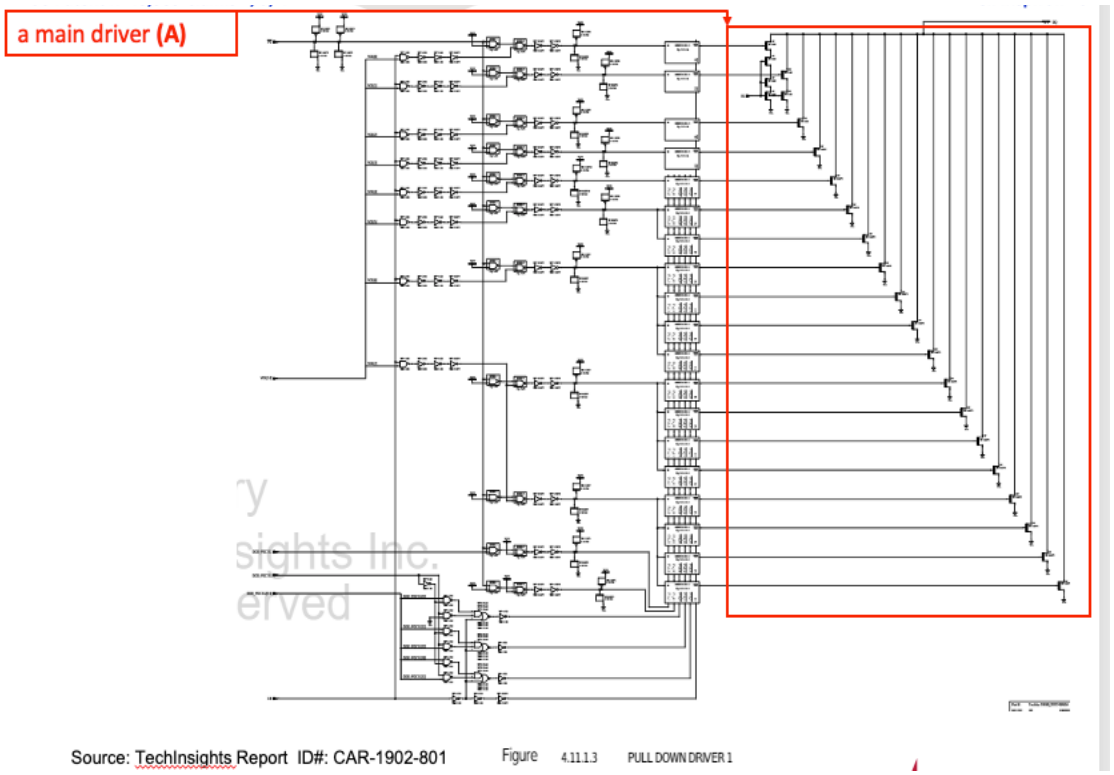
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11 DATA OUTPUT DRIVERS



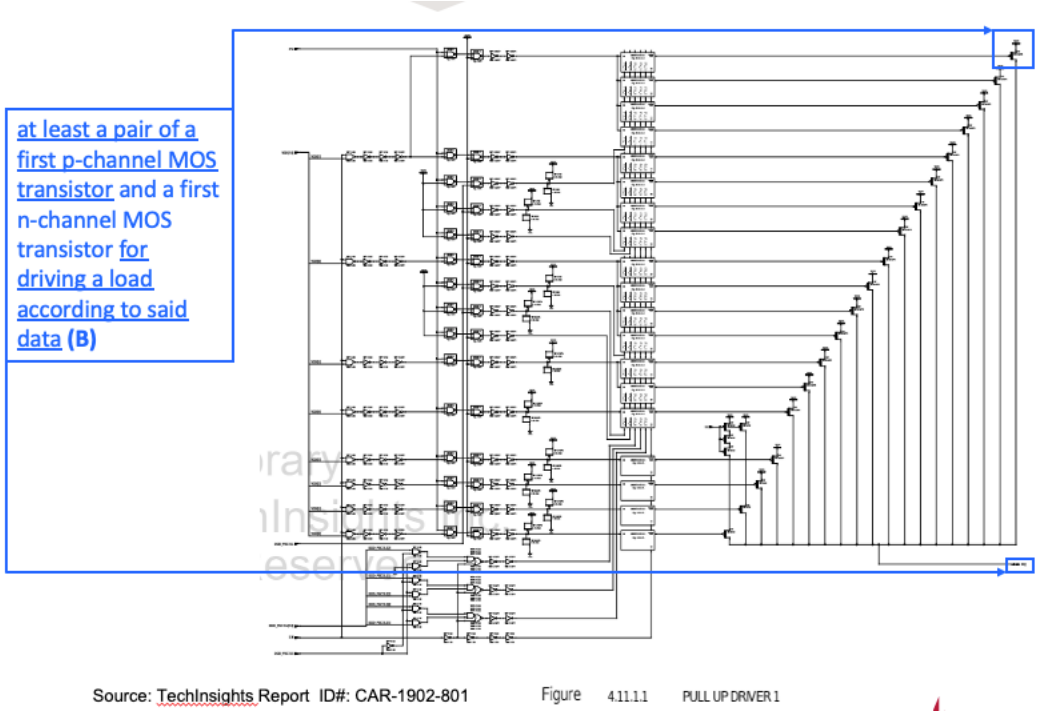
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1 DATA OUTPUT DRIVER

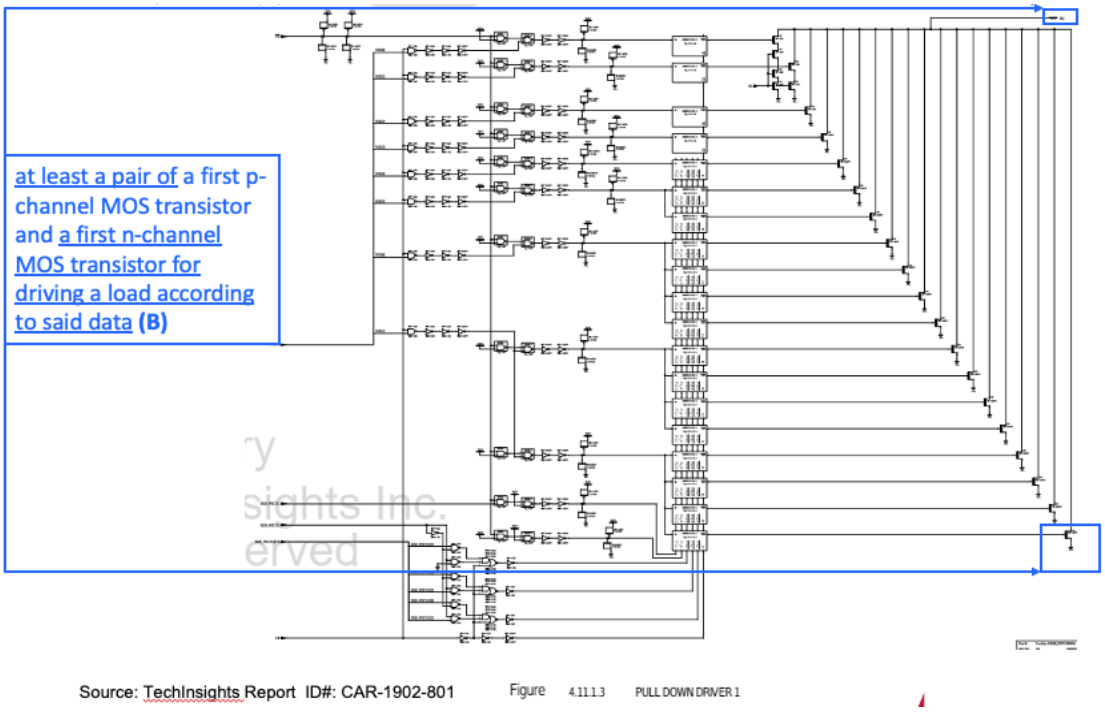


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1



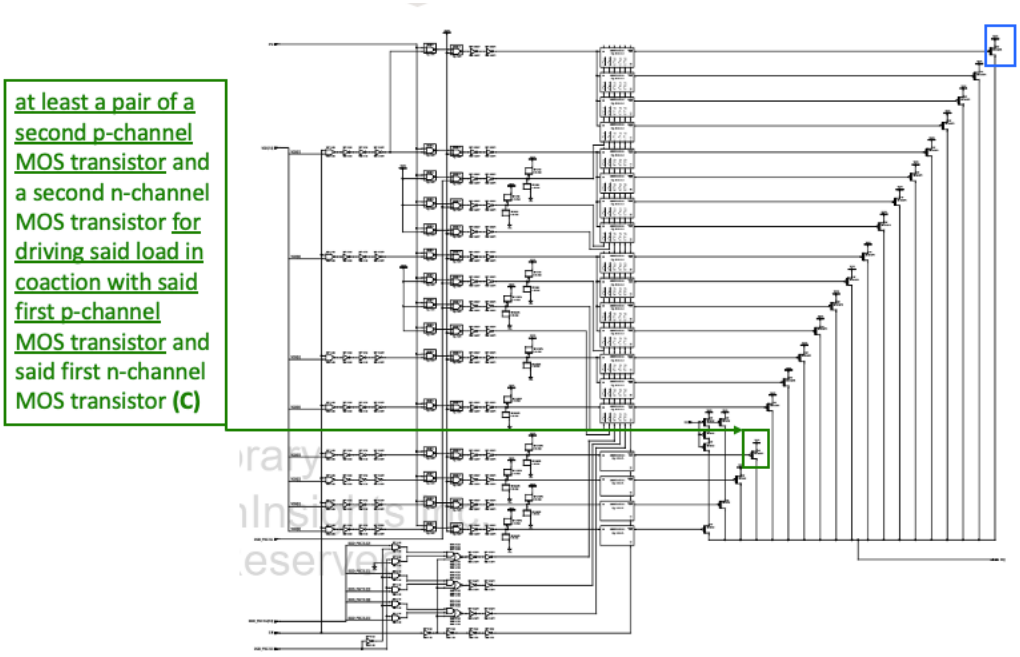
64. The Western Digital PC SN530 NVMe SSD further includes at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data:



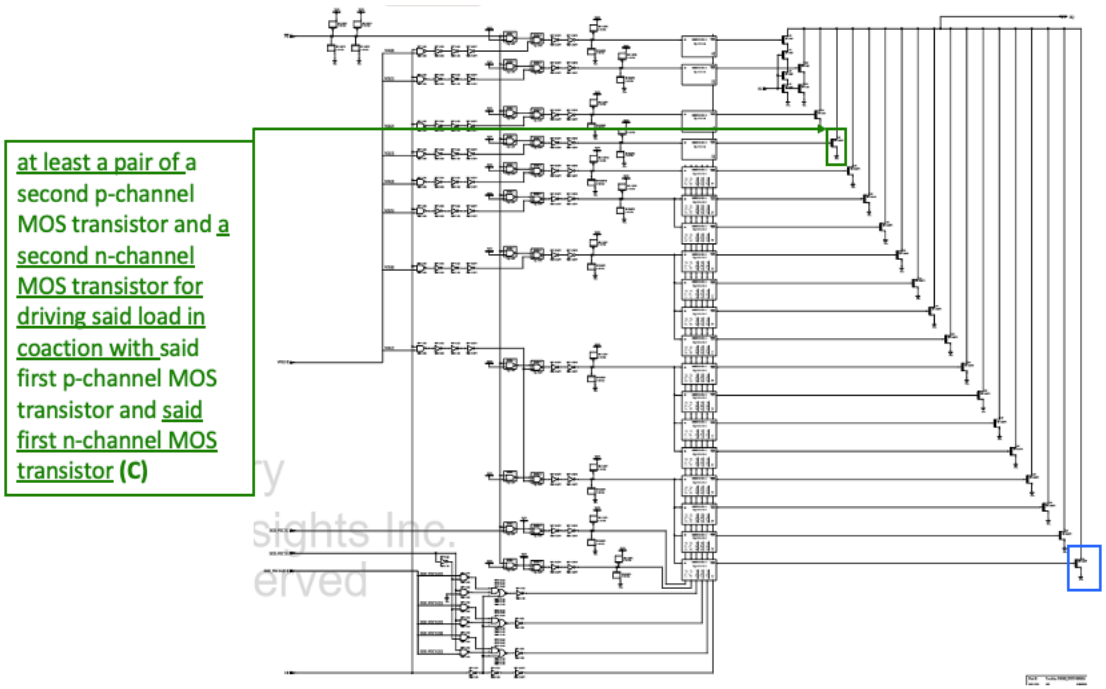


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

65. The Western Digital PC SN530 NVMe SSD further includes at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor:

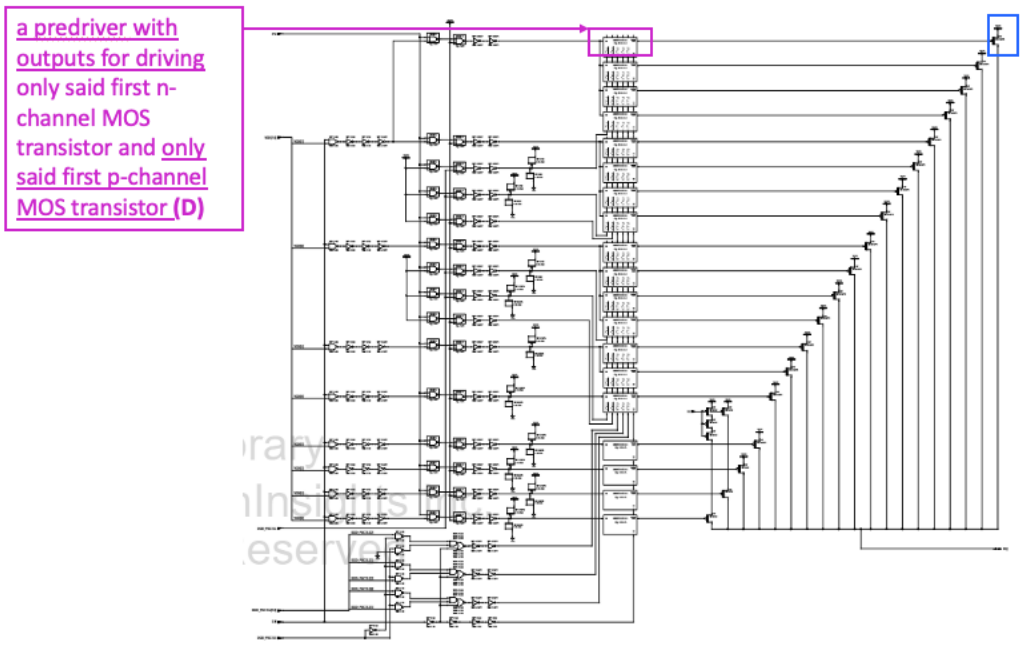


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

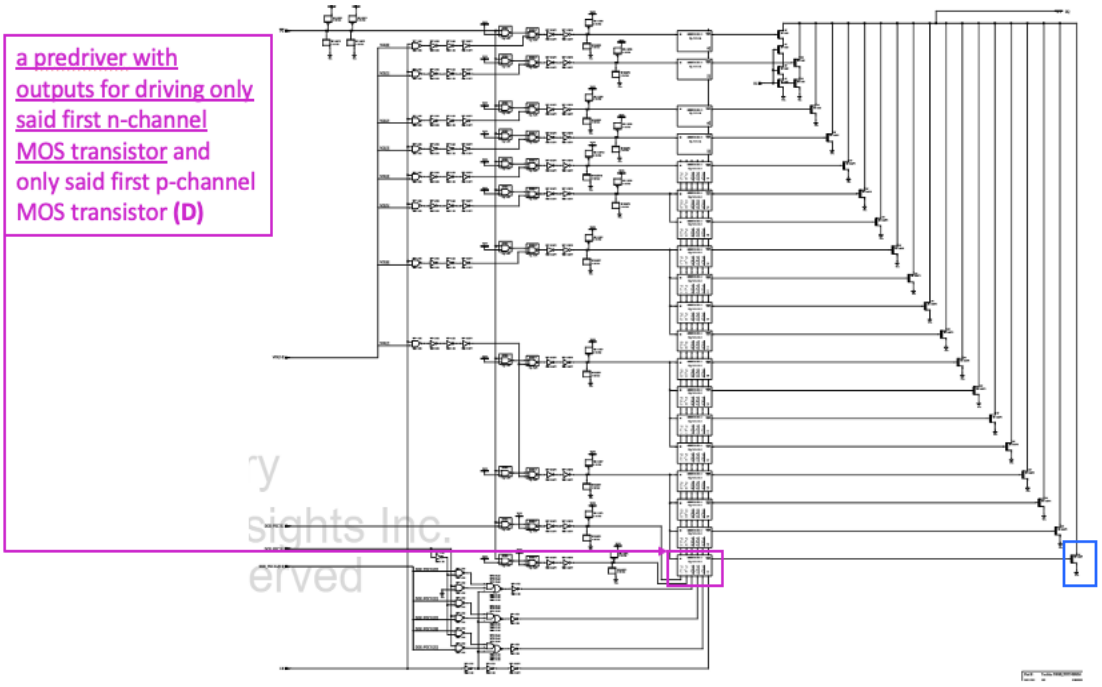


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

66. The Western Digital PC SN530 NVMe SSD includes a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor:

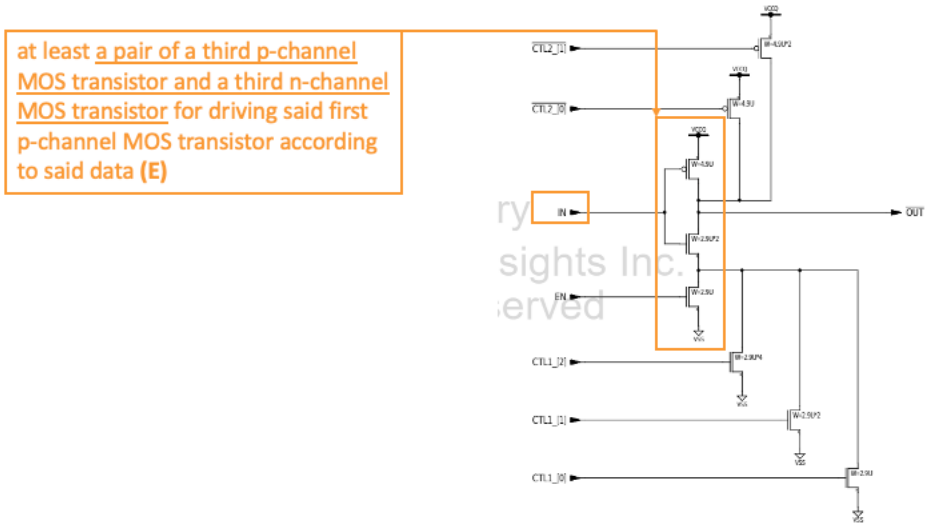


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

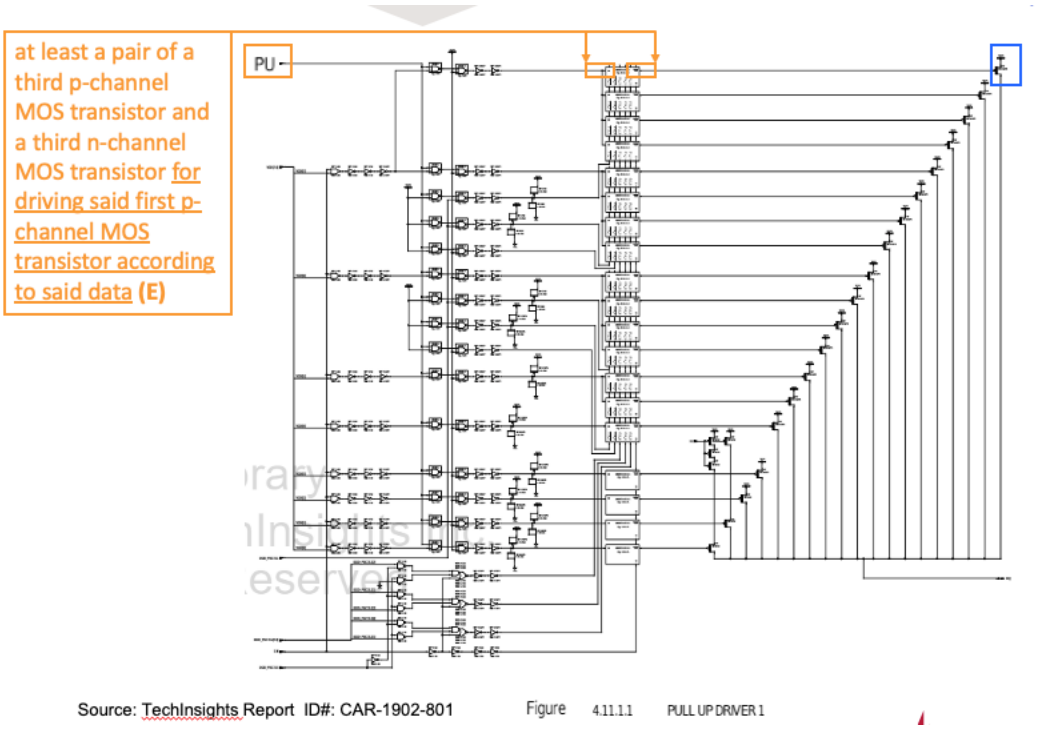


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

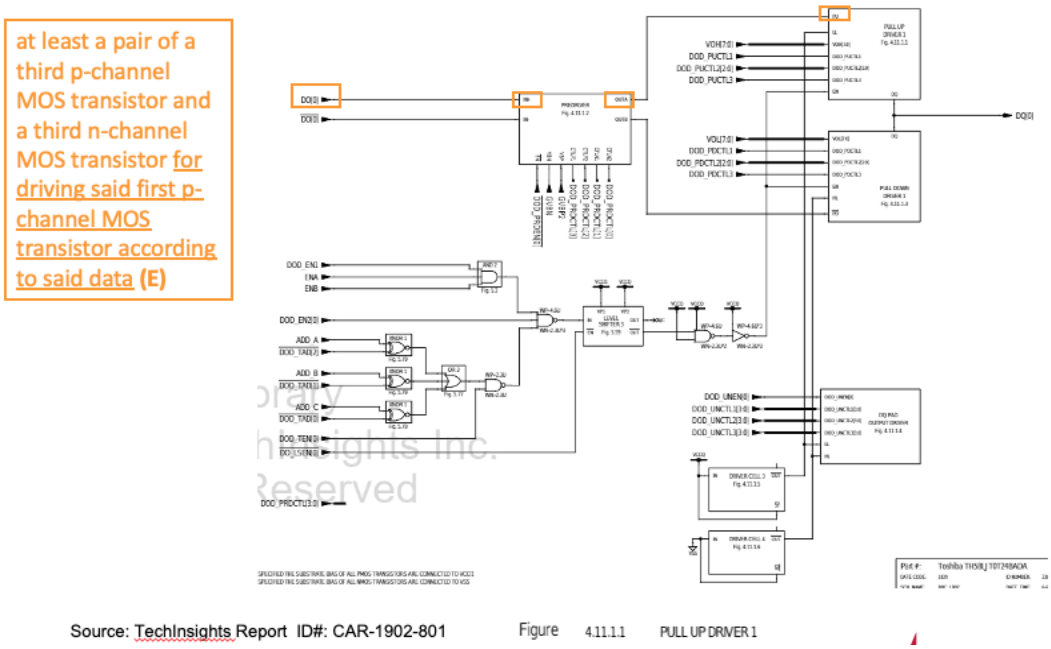
67. The Western Digital PC SN530 NVMe SSD further comprises at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data:



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1.1 DRIVER CELL 1



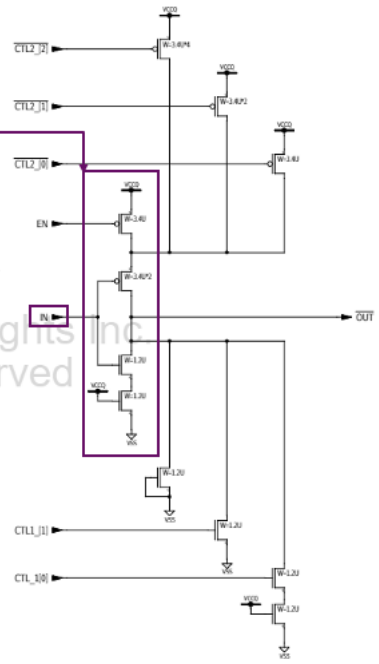
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

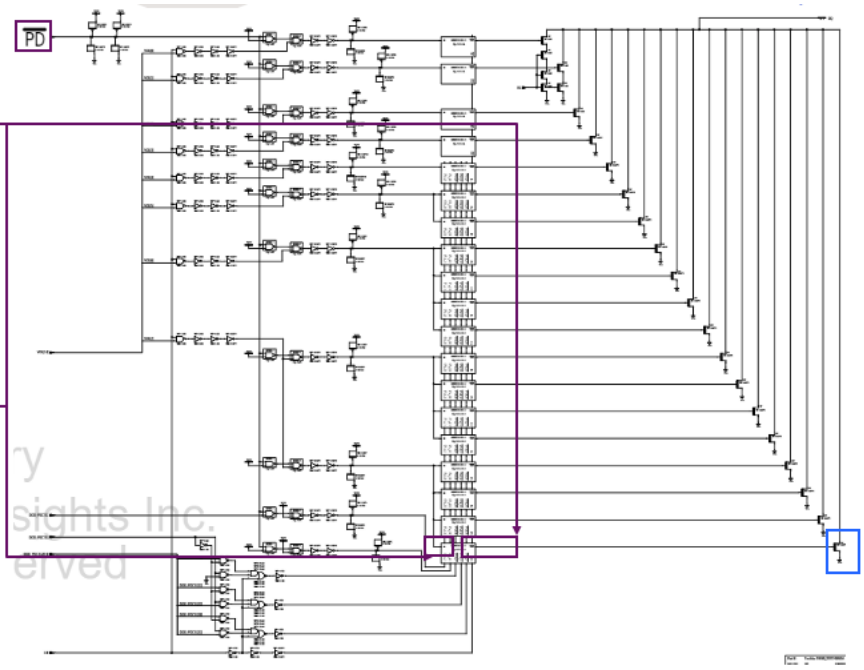
68. The Western Digital PC SN530 NVMe SSD further includes at least a pair of fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data:

at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data **(F)**

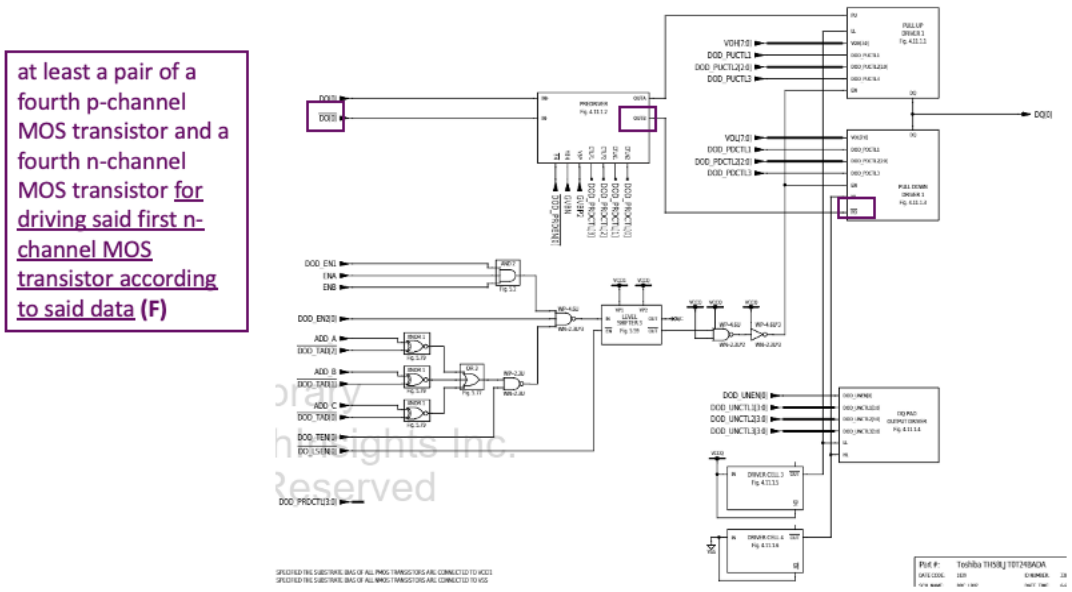


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2

at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data **(F)**

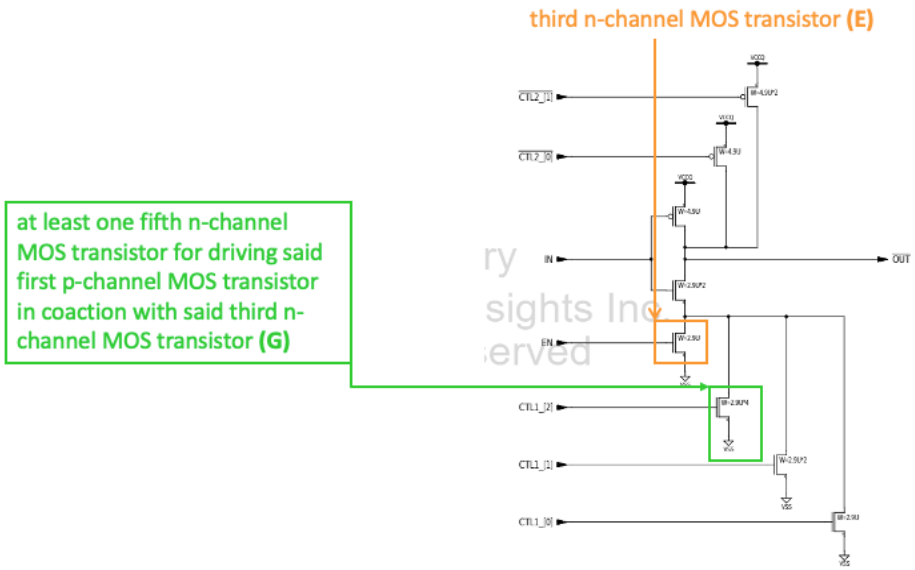


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1



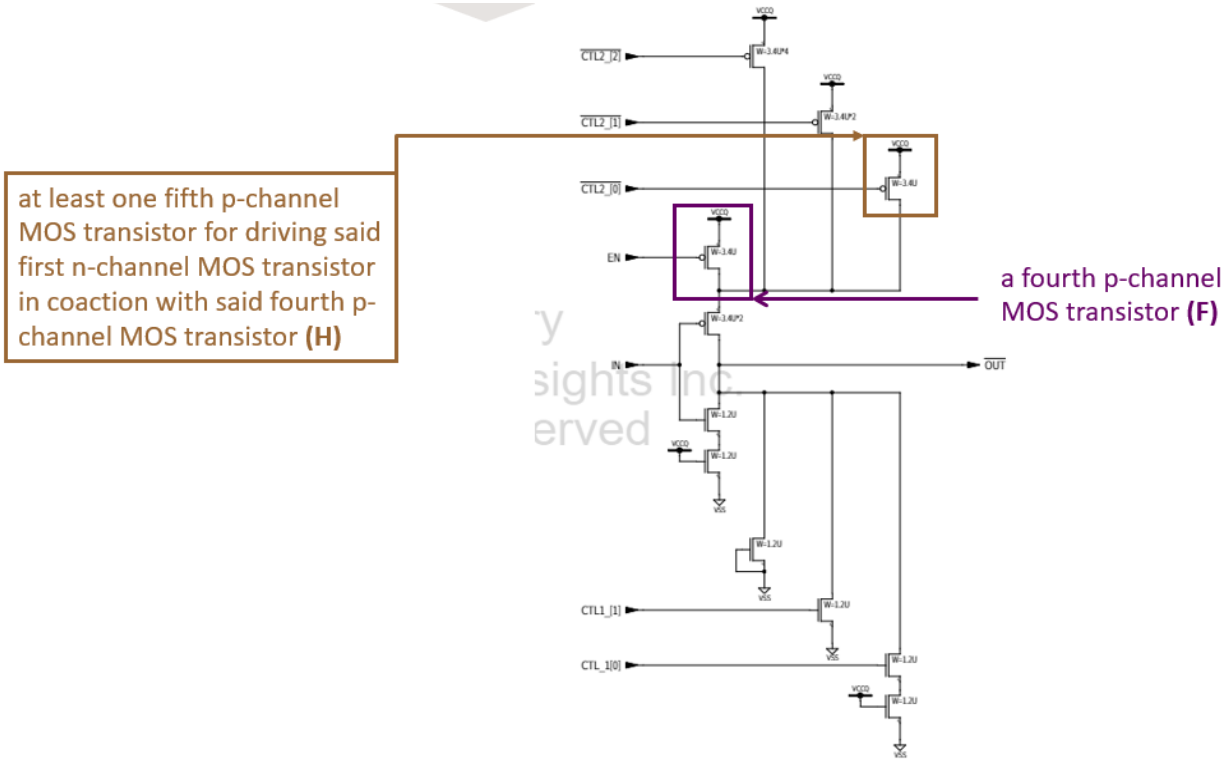
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

69. The Western Digital PC SN530 NVMe SSD further includes at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor:



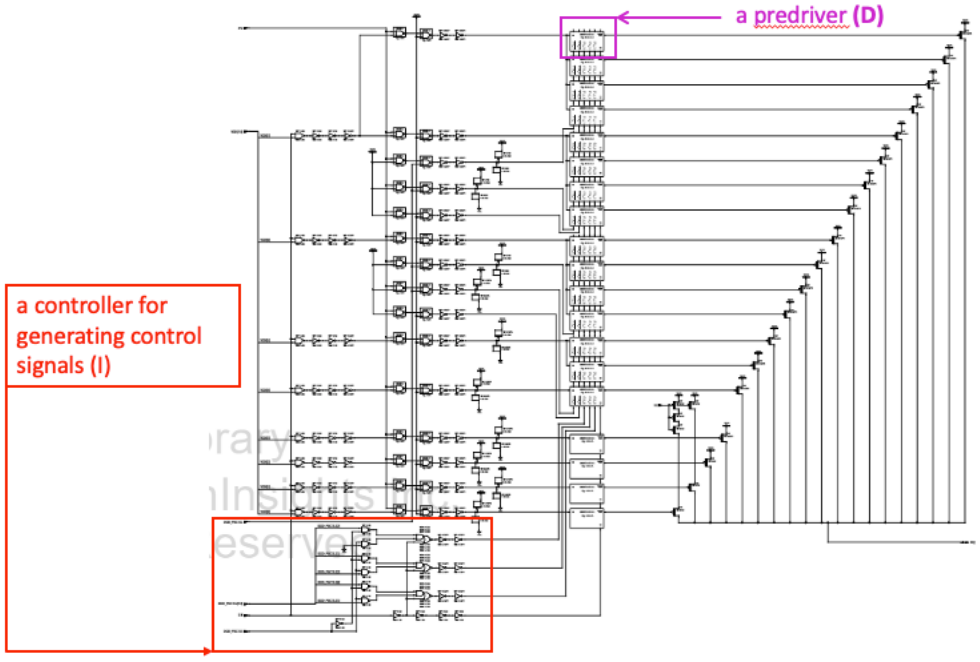
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1.1 DRIVER CELL 1

70. The Western Digital PC SN530 NVMe SSD further includes at least one fifth p-channel MOS transistor in coaction with said fourth p-channel MOS transistor:

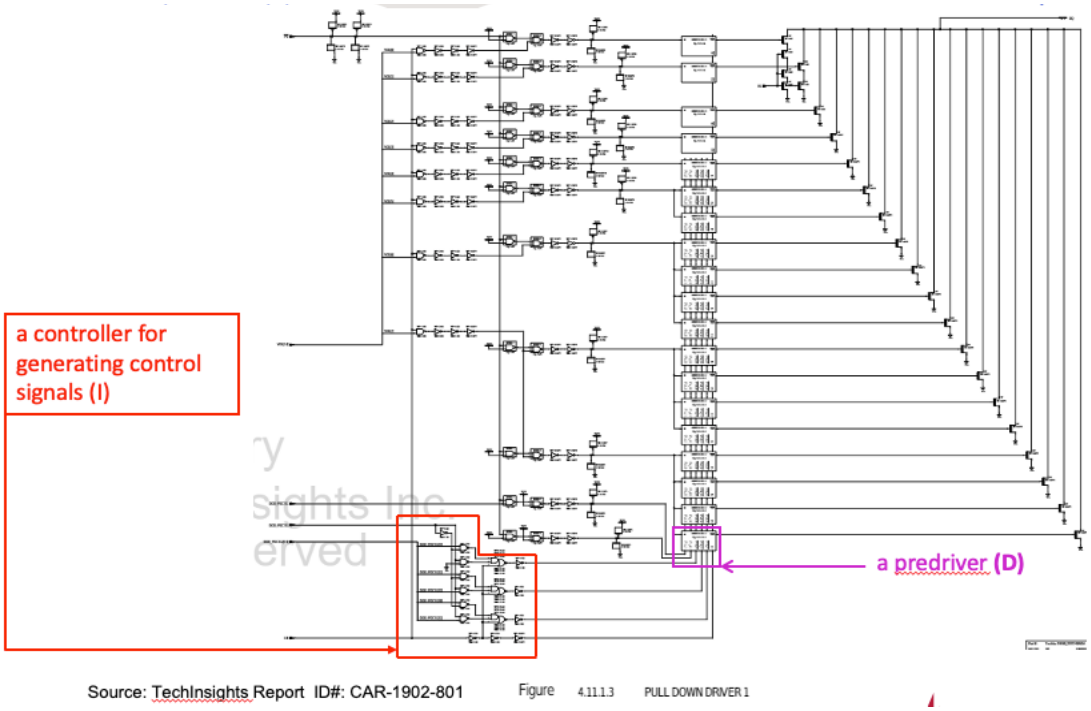


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2

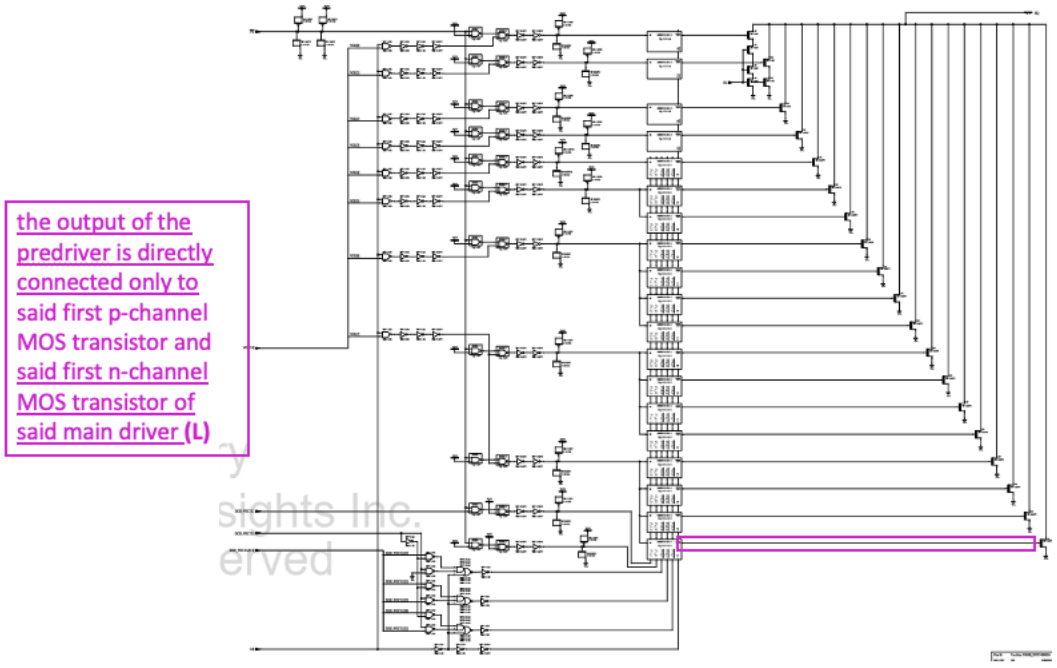
71. The Western Digital PC SN530 NVMe SSD further includes a controller for generating control signals:



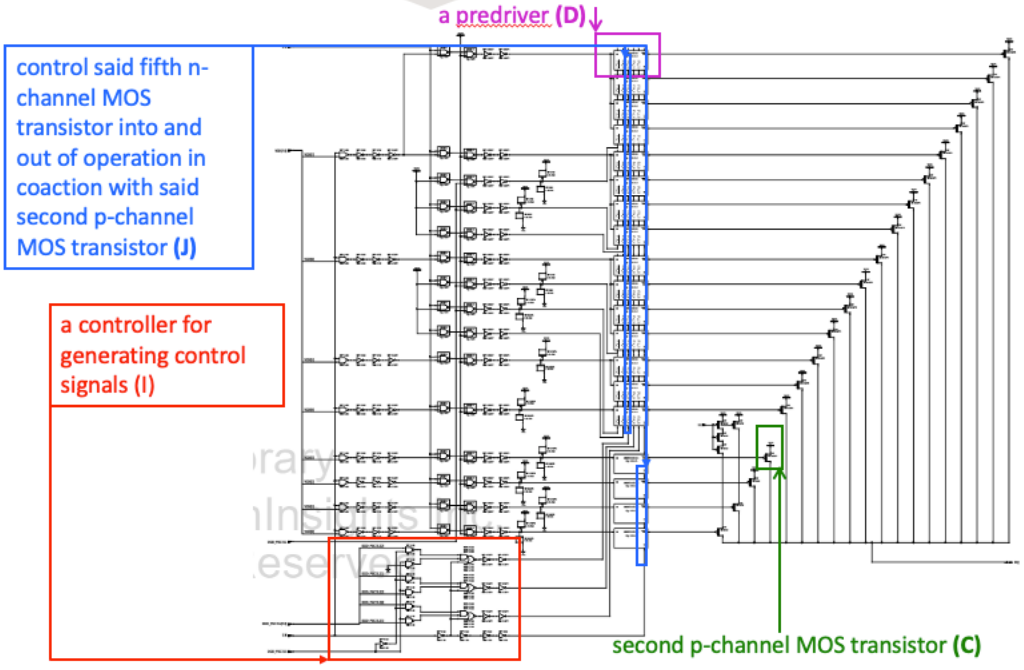
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1



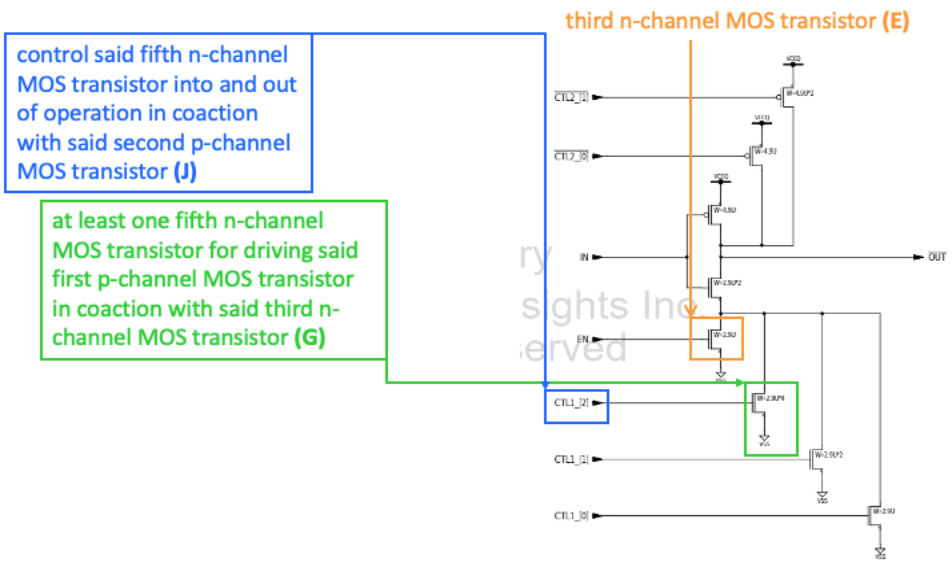
72. The Western Digital PC SN530 NVMe SSD further includes a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor:



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

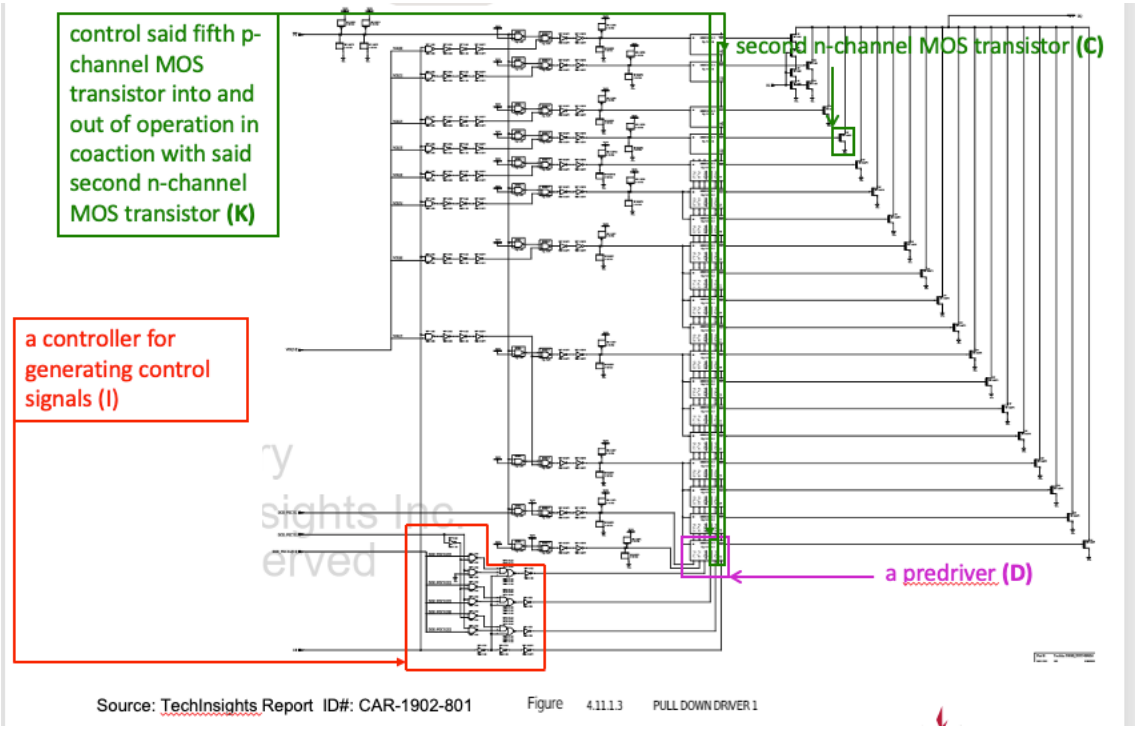


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

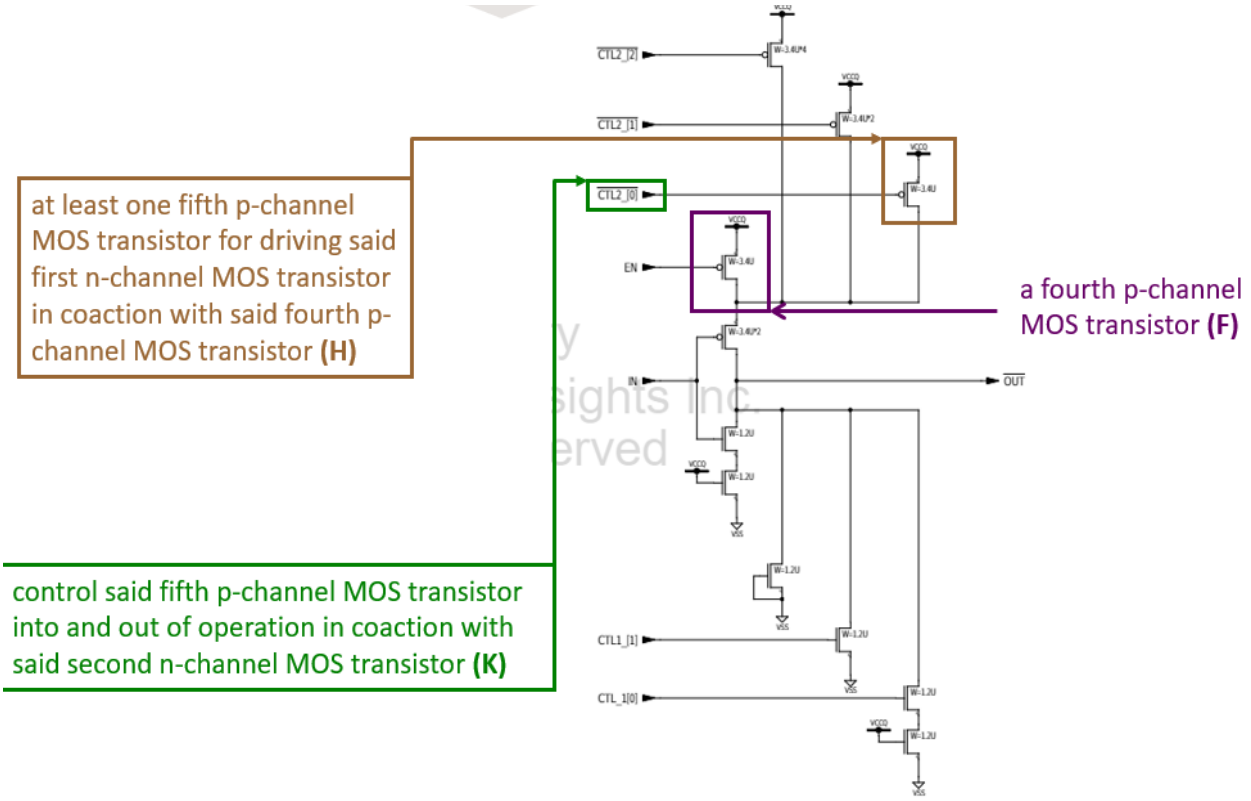


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1.1 DRIVER CELL 1

73. The Western Digital PC SN530 NVMe SSD further includes a controller for generating control signals to control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS-transistor:

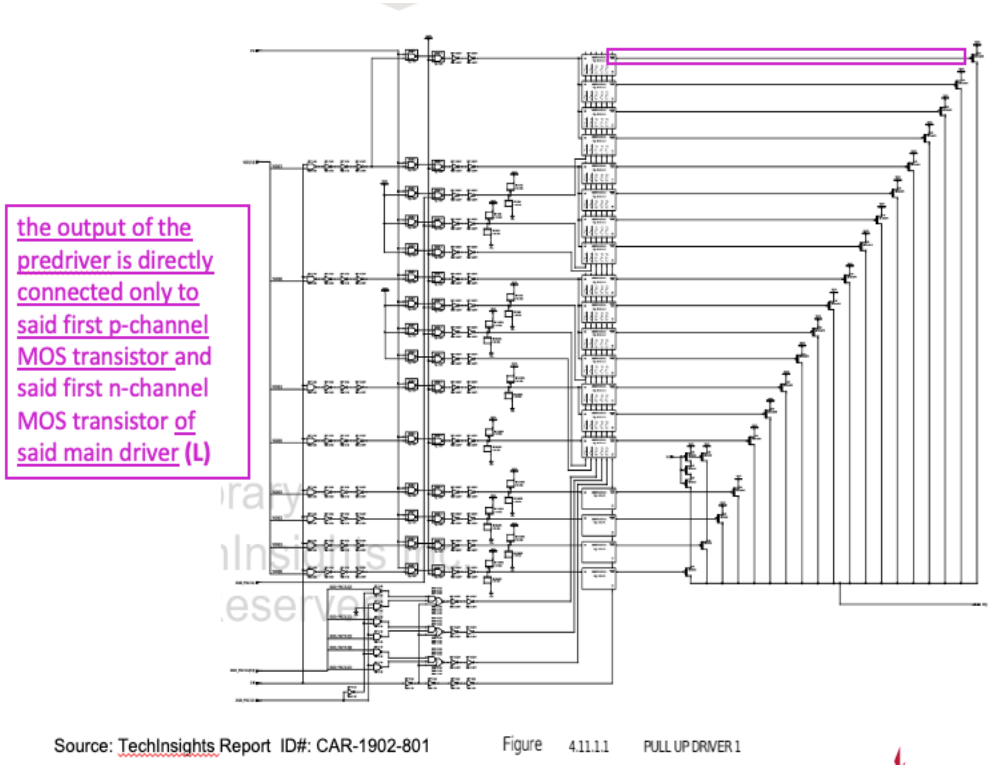


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2

74. The Western Digital PC SN530 NVMe SSD further includes a controller wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver:



75. Defendant actively, knowingly, and intentionally induces, and continues to actively, knowingly, and intentionally induce, infringement of the '539 patent under 35 U.S.C. §271(b) by its customers and end users.

76. Defendant has had knowledge of and notice of the '539 patent and its infringement since at least the filing of this complaint.

77. Defendant has induced its customers and end users to infringe the '539 patent by using their products as shown above. For example, Defendant encourages its customers and end users to perform infringing methods by the very nature of the products.

78. Defendant specifically intends its customers and/or end users infringe the '539 patent, either literally or by the doctrine of equivalents, because Defendant has known about the '539 patent and how Defendant's products infringe the claims of the '539 patent but Defendant has not taken steps to prevent infringement by its customers and/or end users. Accordingly, Defendant has acted with the specific intent to induce infringement of the '539 patent.

79. Accordingly, Defendant has induced, and continues to induce, infringement of the '539 patent under 35 U.S.C. §271(b).

80. As discussed above, Defendant has had knowledge of and notice of the '539 patent and its infringement since at least the filing of this Complaint. Despite this knowledge, Defendant continues to commit tortious conduct by way of patent infringement.

81. Defendant has been and continues to infringe one or more of the claims of the '539 patent through the aforesaid acts.

82. Defendant has committed these acts of infringement without license or authorization.

83. Plaintiff is entitled to recover damages adequate to compensate for the infringement.

84. Defendant has and continues to infringe the '539 patent, acting with an objectively high likelihood that its actions constitute infringement of the '539 patent. Defendant has known or should have known of this risk at least as early as the filing of this Complaint. Accordingly, Defendant's infringement of the '539 patent has been and continues to be willful.

COUNT III

(DEFENDANT'S INFRINGEMENT OF THE '233 PATENT)

85. Paragraphs 1 through 84 are incorporated by reference as if fully restated herein.

86. United States Patent No. 9,379,233, entitled "Semiconductor Device," issued on June 28, 2016 from United States Patent Application No. 14/872,844 filed October 1, 2015.

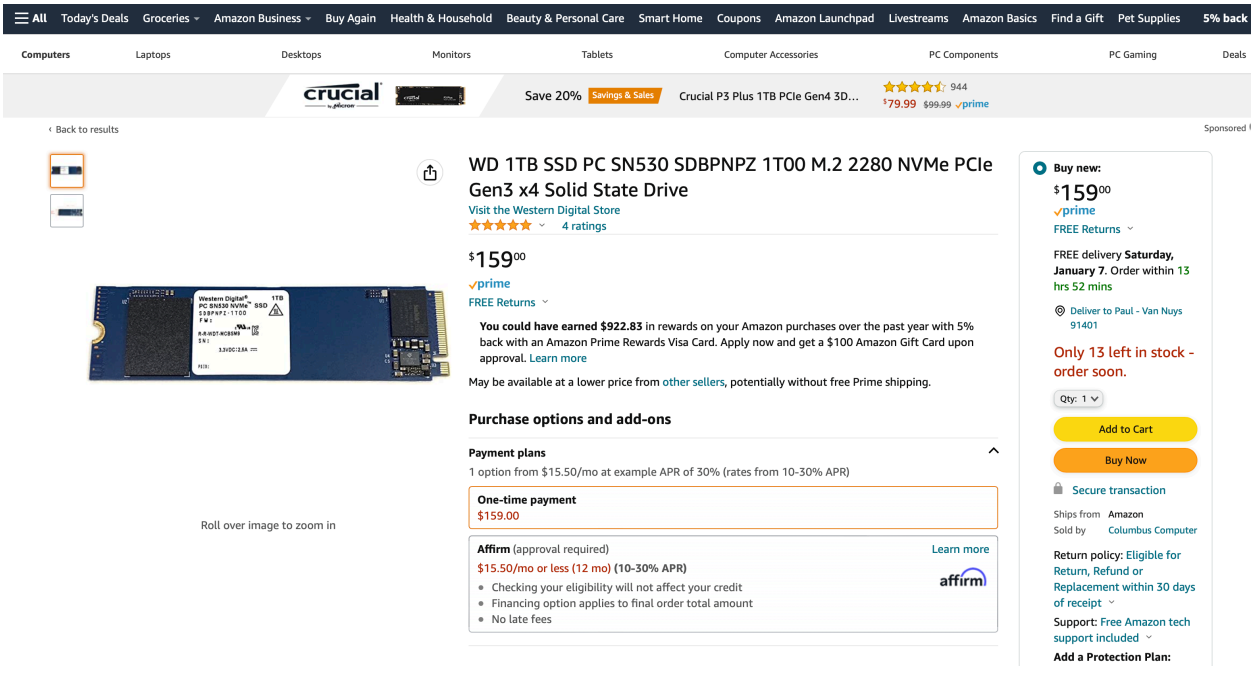
87. Longitude is the owner of the '233 patent with full rights to pursue recovery of royalties for damages for infringement, including full rights to recover past and future damages.

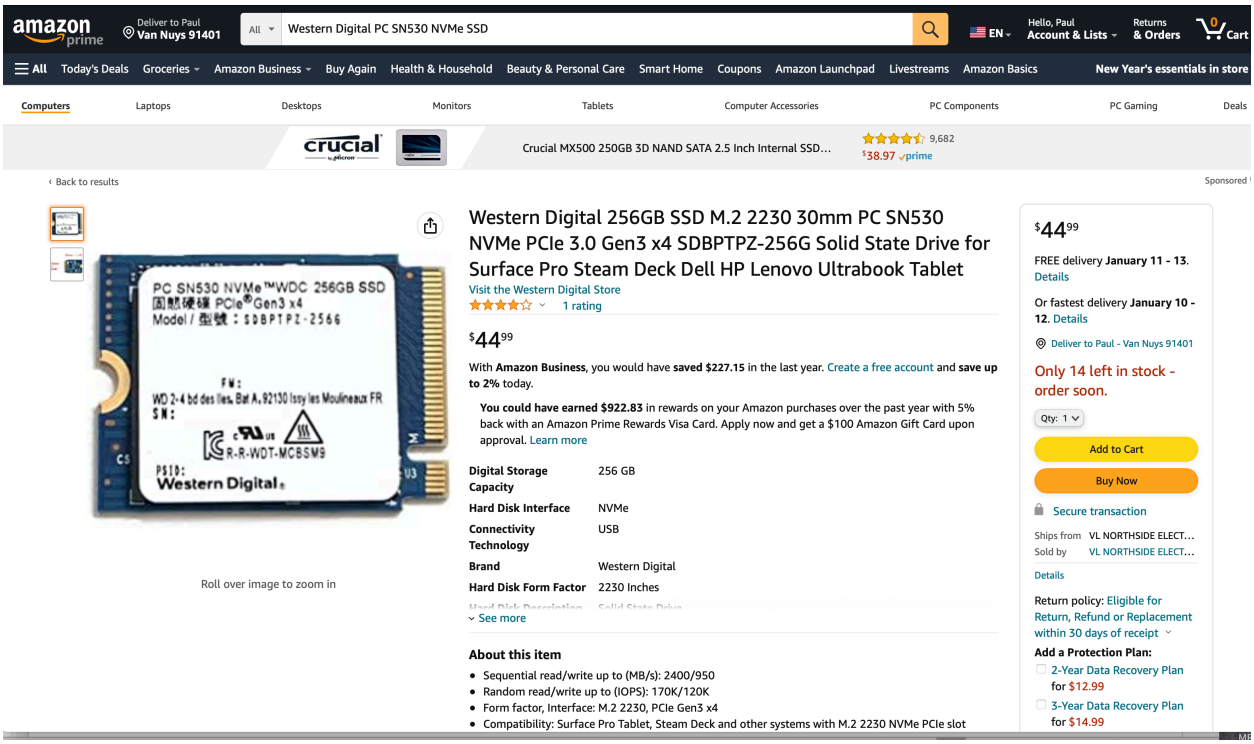
88. Each claim of the '233 patent is valid, enforceable, and patent-eligible.

89. Longitude and its predecessors in interest have satisfied the requirements of 35 U.S.C. § 287(a) with respect to the '233 patent, and Longitude is entitled to damages for Defendant's past infringement. Among other things, Longitude provided actual notice of infringement to the component supplier, Western Digital.

90. Defendant has directly infringed (literally and equivalently) and induced others to infringe the '233 patent by making, using, selling, offering for sale, or importing products that infringe the claims of the '233 patent and by inducing others to infringe the claims of the '233 patent without a license or permission from Longitude. These products include without limitation Western Digital PC SN530 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the '233 patent.

91. A non-limiting example of Defendant's infringement is its sales and offers for sale of Western Digital PC SN530 NVMe SSDs as demonstrated below.

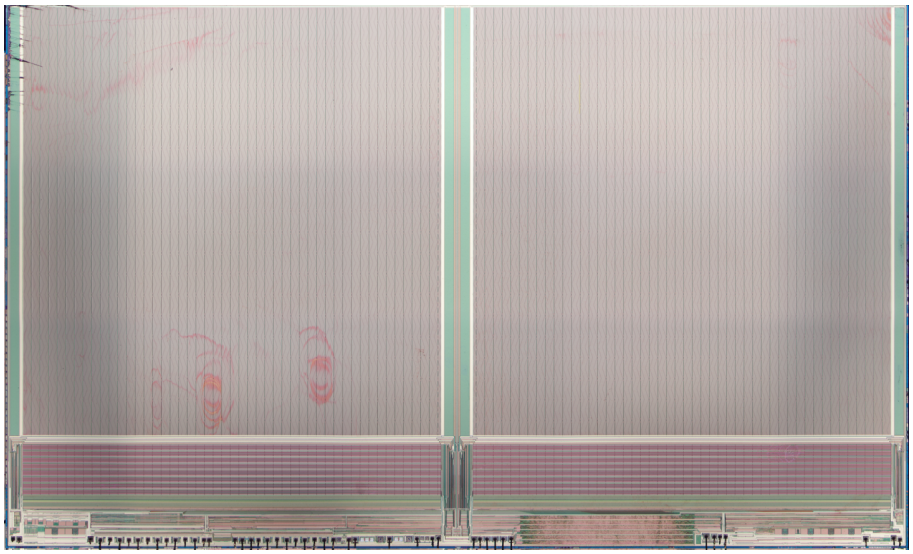




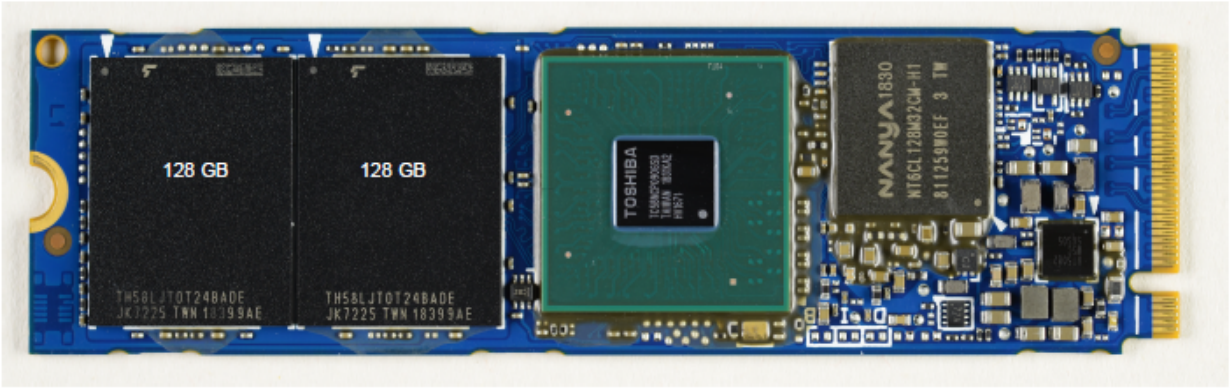
92. Western Digital PC SN530 NVMe SSDs infringe at least claim 1 of the '233 patent.

93. The Western Digital PC SN530 NVMe SSD includes a SanDisk memory chip as shown below:

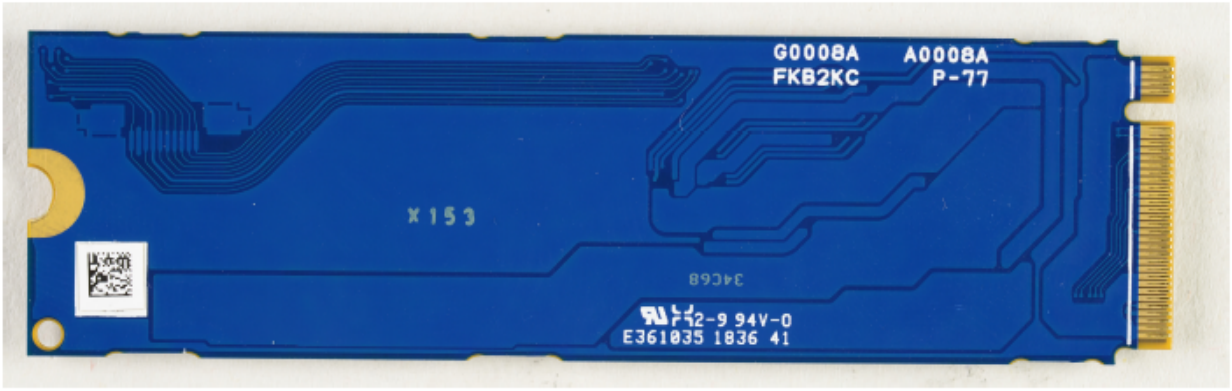
94. The below image shows the pin layout and corners of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD:



95. On information and belief, the Western Digital PC SN530 NVMe SSD is substantially similar to the Toshiba KXG60ZNV256G SSD Package ("Toshiba SSD") for all matters relevant to this complaint. The Toshiba SSD is depicted below:

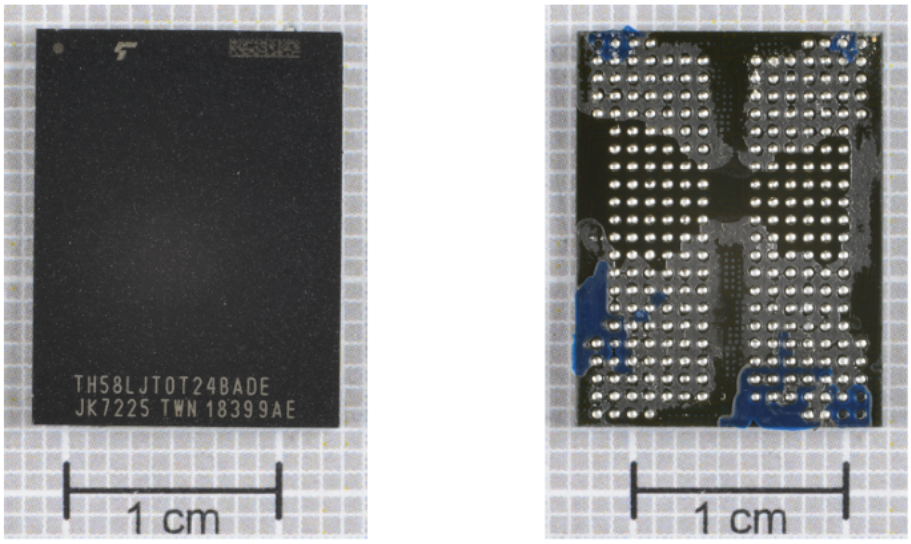


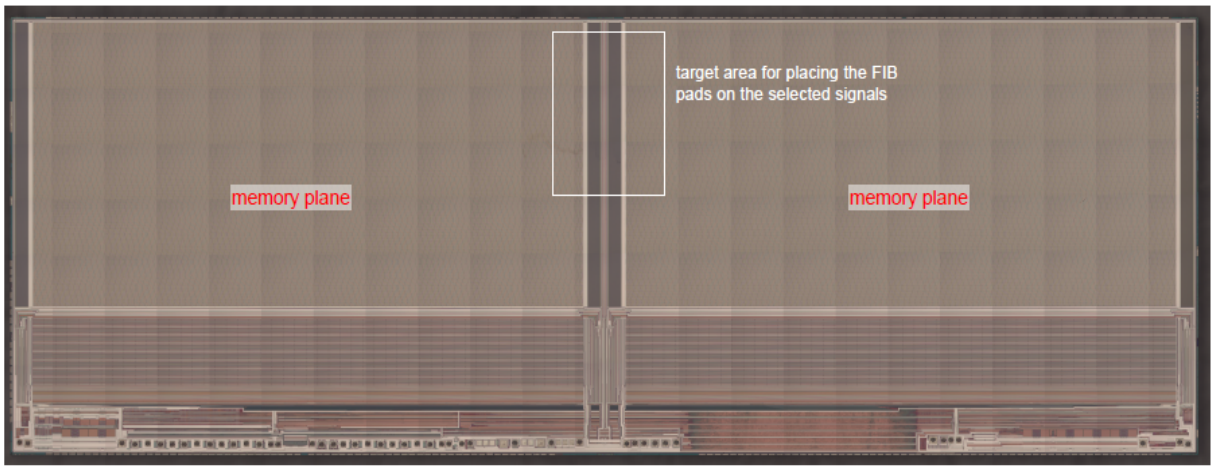
Toshiba KXG60ZNV256G SSD Package – Top



Toshiba KXG60ZNV256G SSD Package – Bottom

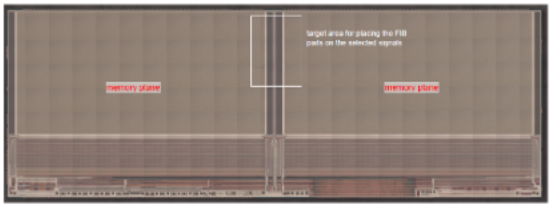
96. The memory chip of the Toshiba SSD, the Toshiba TH58LJT0T24BADE Package, is depicted in the images below:



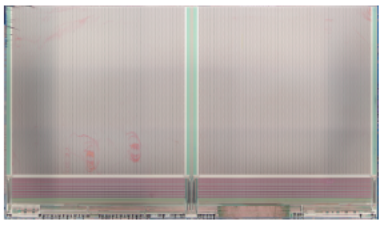


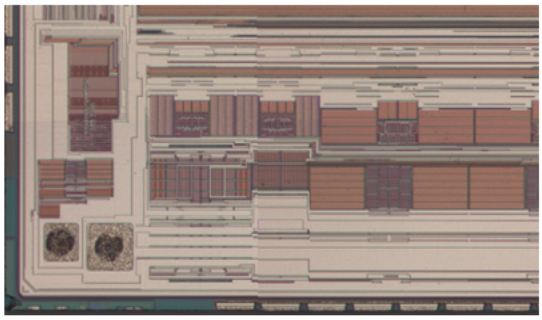
Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

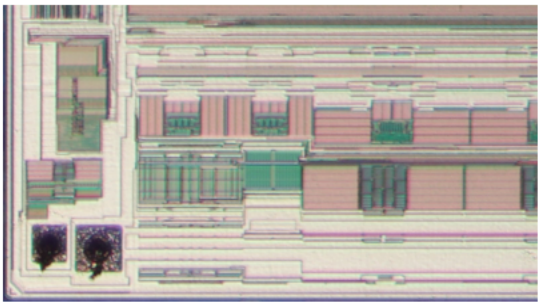
97. A side-by-side comparison of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package used in the Toshiba SSD is depicted below:



Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

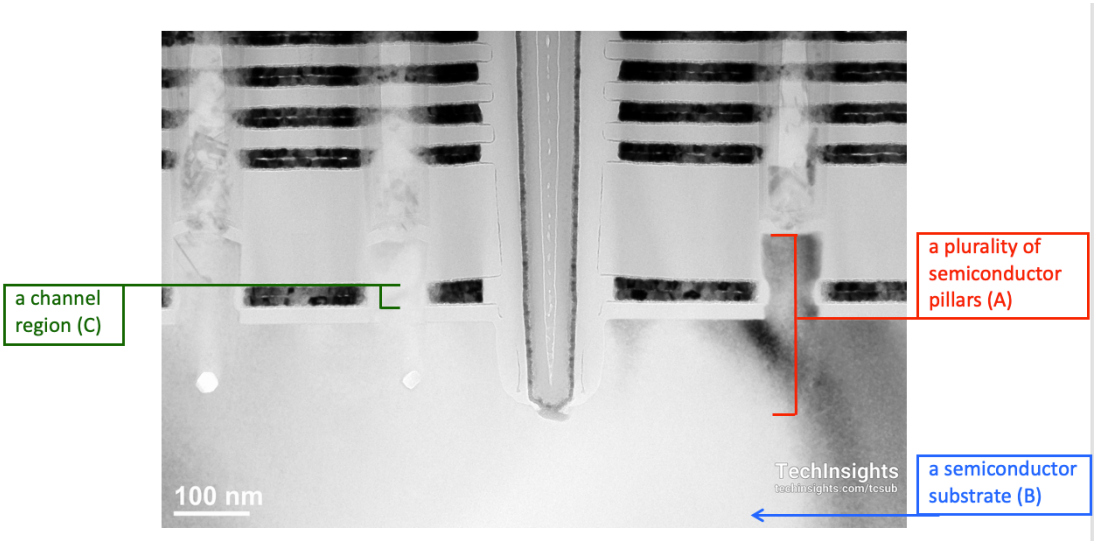


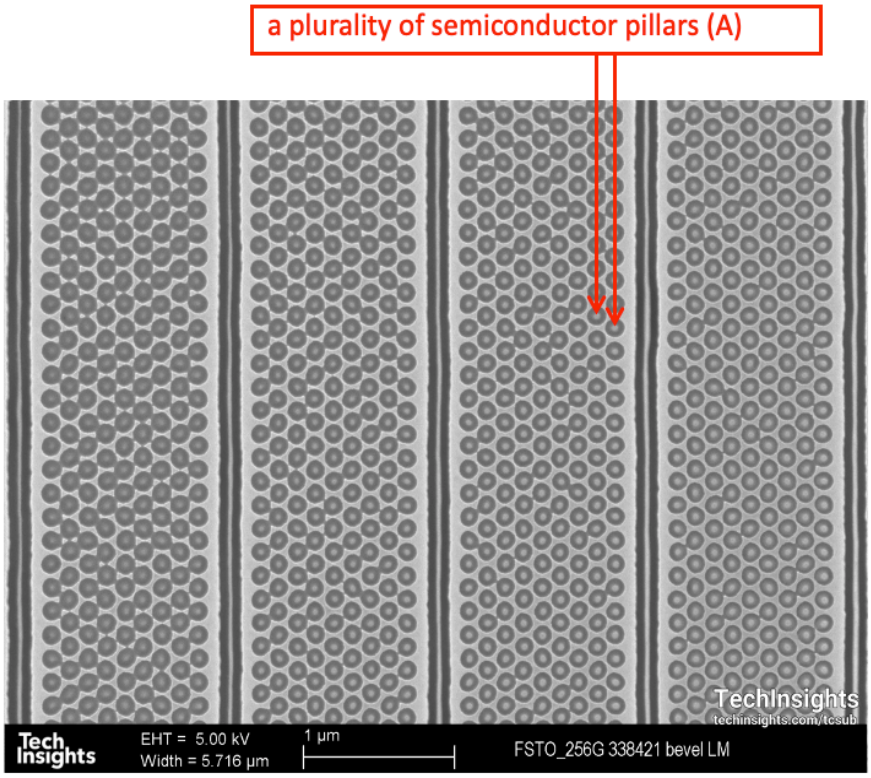




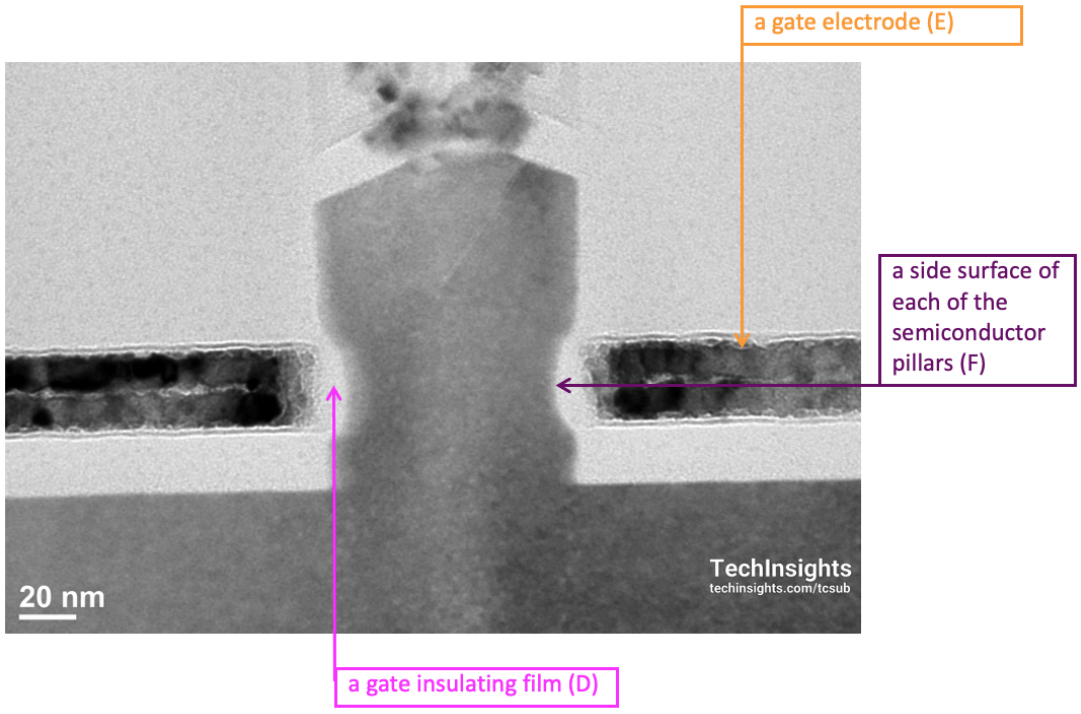
98. Based at least on the above, Longitude is informed and believes that the corners of the dies of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package are substantially the same. Accordingly, Longitude is informed and believes that the various I/Os and peripheral circuits are the same between the Toshiba and Western Digital/SanDisk chips. Furthermore, Longitude is informed and believes that Toshiba and Western Digital shared the designs for 96 layer chips. As shown above, the SanDisk memory chip is substantially the same as the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package. For this reason, Longitude is informed and believes that technical documents and other analysis concerning the Toshiba TH58LJT0T24BADE Package also describe the layout and functionality of the Western Digital PC SN530 NVMe SSD and the SanDisk memory chip therein.

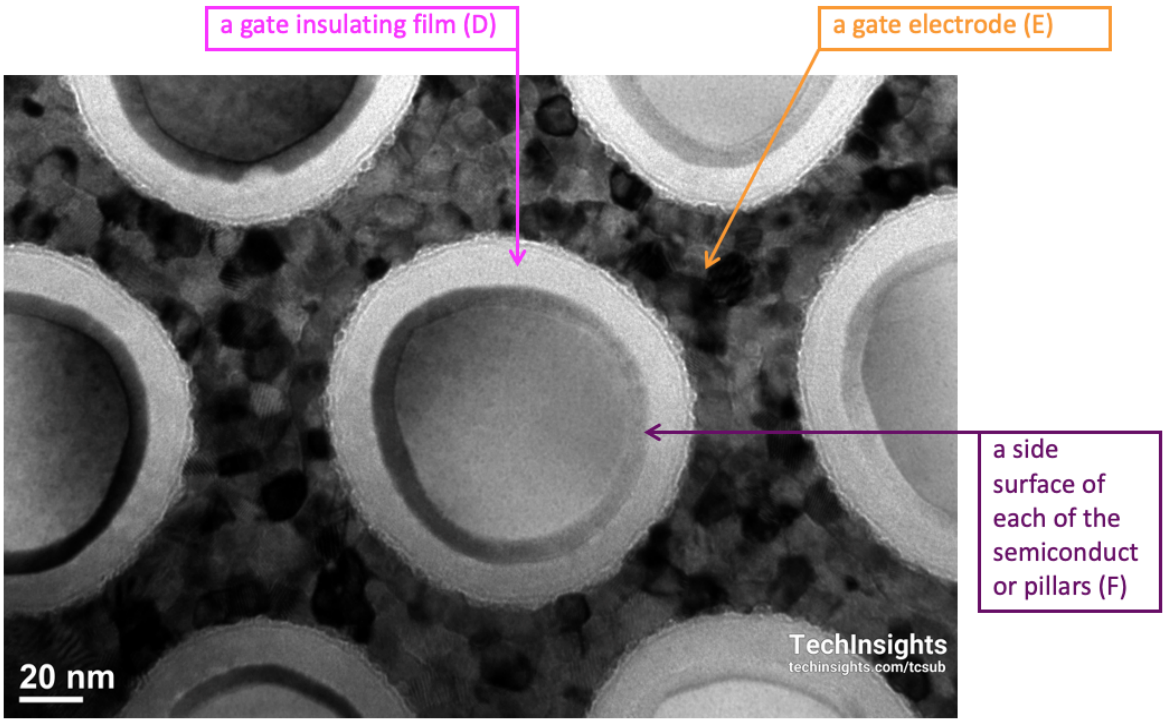
99. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region:



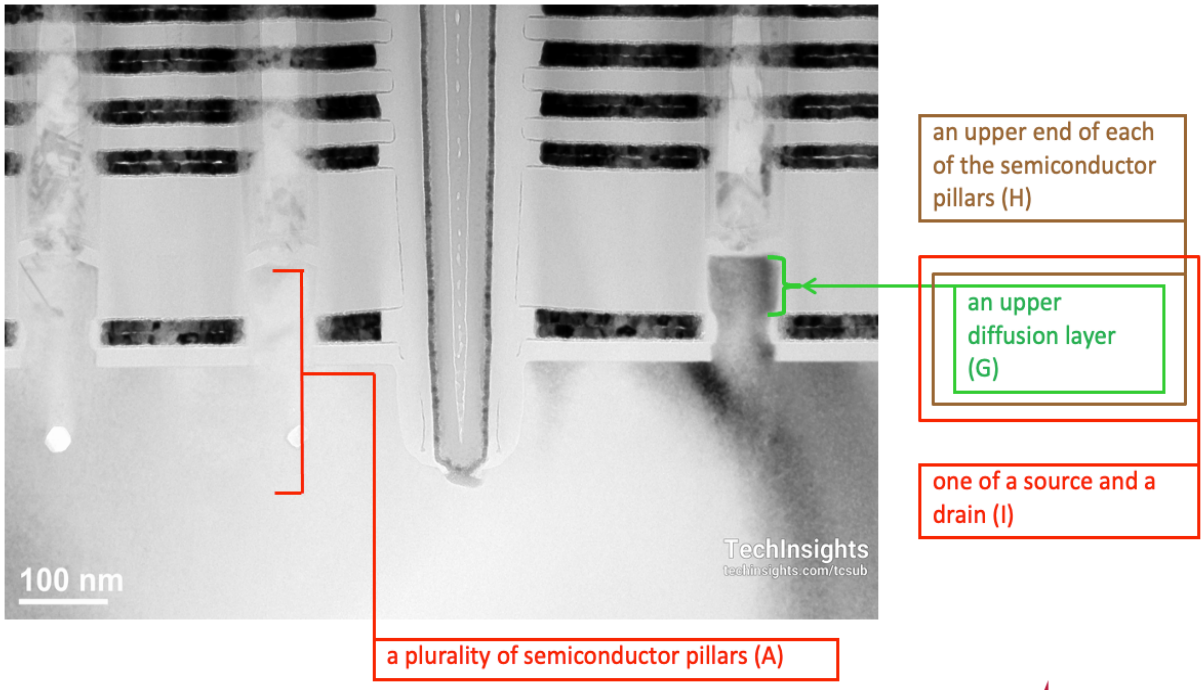


100. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars:

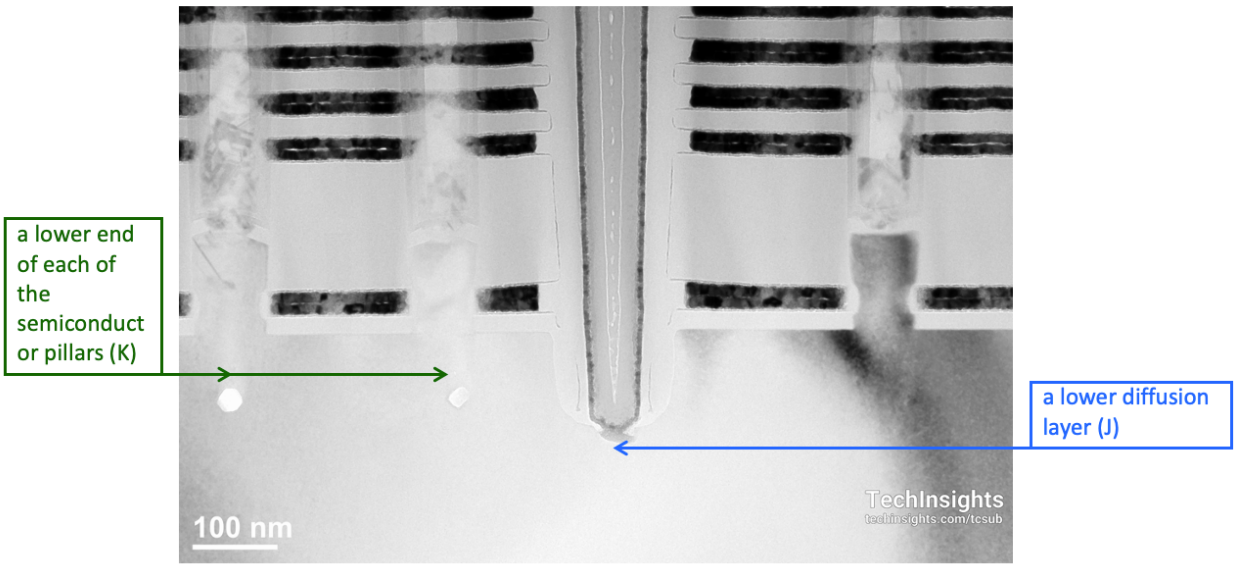




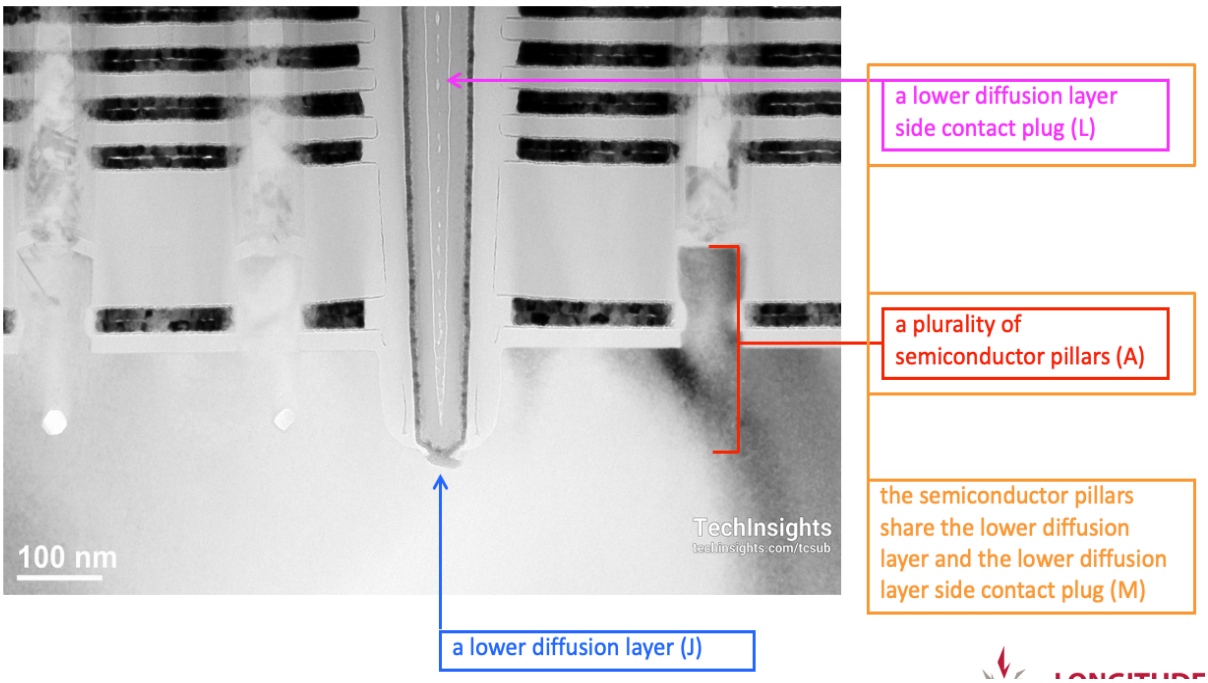
101. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain:



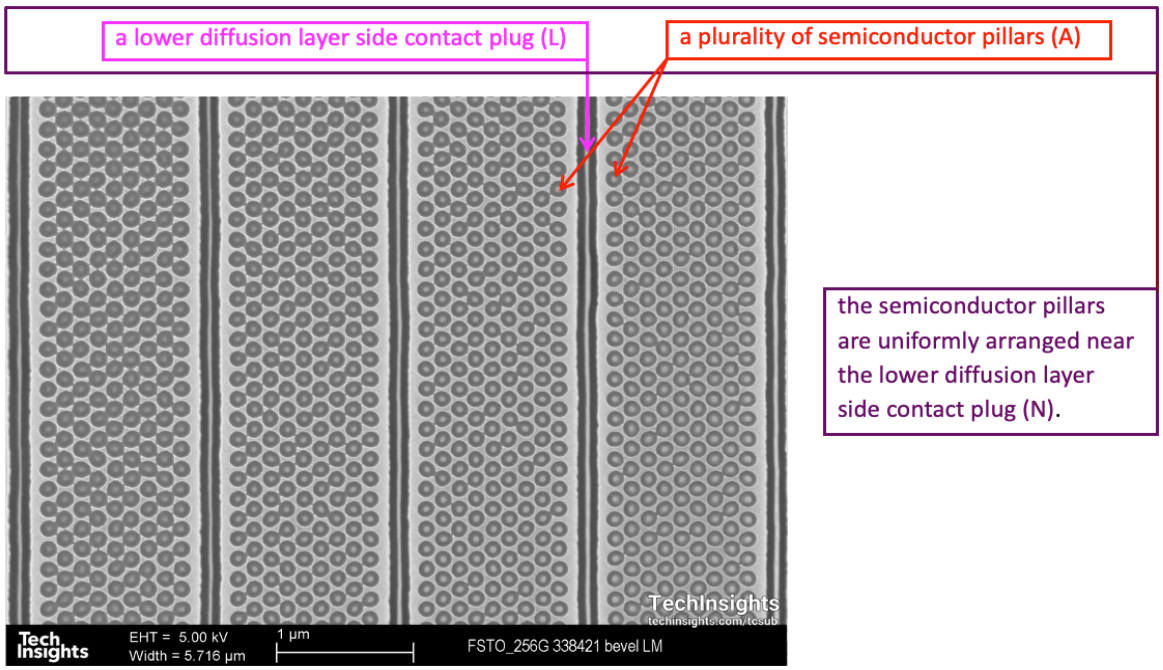
102. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain:



103. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug:



104. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device wherein the semiconductor pillars are uniformly arranged near the lower diffusion side contact:



105. Defendant actively, knowingly, and intentionally induces, and continues to actively, knowingly, and intentionally induce, infringement of the ’233 patent under 35 U.S.C. §271(b) by its customers and end users.

106. Defendant has had knowledge of and notice of the ’233 patent and its infringement since at least the filing of this complaint.

107. Defendant has induced its customers and end users to infringe the ’233 patent by using their products as shown above. For example, Defendant encourages its customers and end users to perform infringing methods by the very nature of the products.

108. Defendant specifically intends its customers and/or end users infringe the ’233 patent, either literally or by the doctrine of equivalents, because Defendant has known about the ’233 patent and how Defendant's products infringe the claims of the ’233 patent but Defendant has not taken steps to prevent infringement by its customers and/or end users. Accordingly, Defendant has acted with the specific intent to induce infringement of the ’233 patent.

109. Accordingly, Defendant has induced, and continues to induce, infringement of the ’233 patent under 35 U.S.C. §271(b).

110. As discussed above, Defendant has had knowledge of and notice of the '233 patent and its infringement since at the filing of this Complaint. Despite this knowledge, Defendant continues to commit tortious conduct by way of patent infringement.

111. Defendant has been and continues to infringe one or more of the claims of the '233 patent through the aforesaid acts.

112. Defendant has committed these acts of infringement without license or authorization.

113. Plaintiff is entitled to recover damages adequate to compensate for the infringement.

114. Defendant has and continues to infringe the '233 patent, acting with an objectively high likelihood that its actions constitute infringement of the '233 patent. Defendant has known or should have known of this risk at least as early as the filing of this Complaint. Accordingly, Defendant's infringement of the '233 patent has been and continues to be willful.

COUNT IV

(DEFENDANT'S INFRINGEMENT OF THE '701 PATENT)

115. Paragraphs 1 through 114 are incorporated by reference as if fully restated herein.

116. United States Patent No. 9,207,701, entitled "Supply Voltage Generating Circuit," issued on December 8, 2015 from United States Patent Application No. 14/480,768 filed on September 9, 2014.

117. Longitude is the owner of the '701 patent with full rights to pursue recovery of royalties for damages for infringement, including full rights to recover past and future damages.

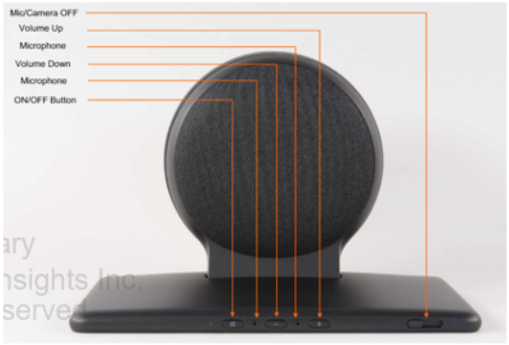
118. Each claim of the '701 patent is valid, enforceable, and patent-eligible.

119. Longitude and its predecessors in interest have satisfied the requirements of 35 U.S.C. § 287(a) with respect to the '701 patent, and Longitude is

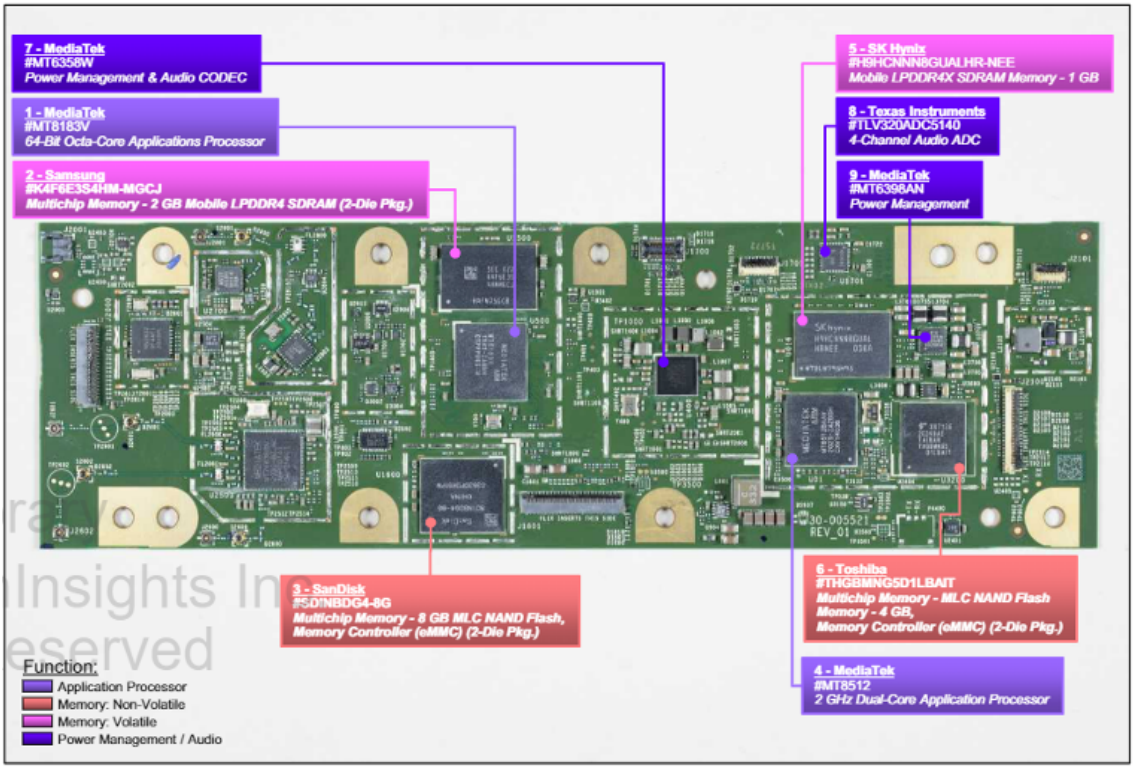
entitled to damages for Defendant's past infringement. Among other things, Longitude provided actual notice of infringement to the component supplier, Western Digital.

120. Defendant has directly infringed (literally and equivalently) and induced others to infringe the '701 patent by making, using, selling, offering for sale, or importing products that infringe the claims of the '701 patent and by inducing others to infringe the claims of the '701 patent without a license or permission from Longitude. These products include without limitation the Amazon Echo Show 10 (*e.g.*, model t4E4AT), Fire TV Stick Lite (*e.g.*, model S3L46N), all other Amazon products having Western Digital FKB7 NAND flash memory and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the '701 patent.

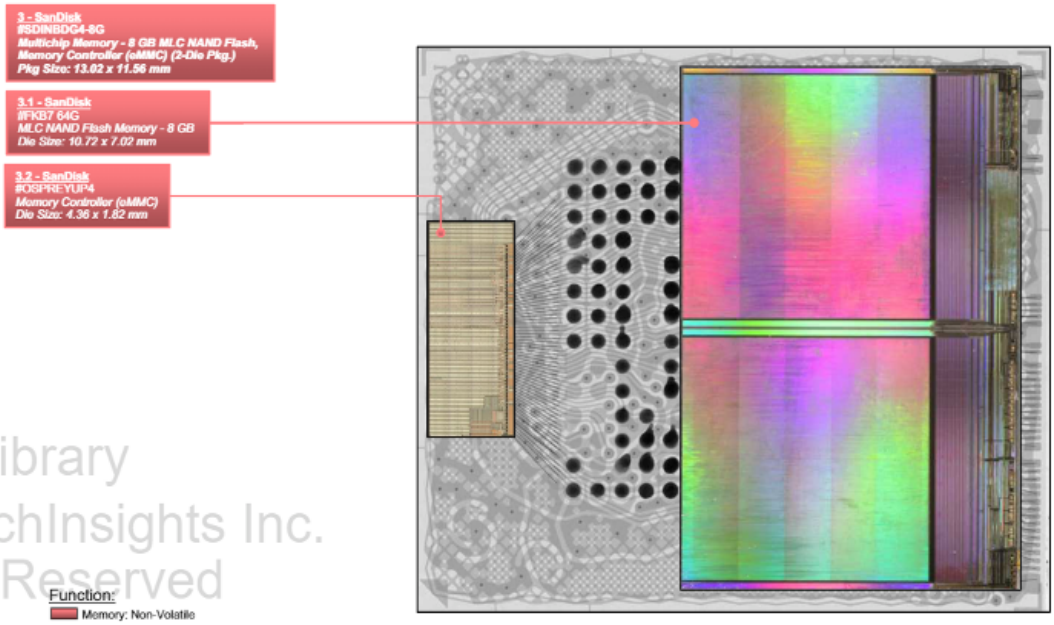
121. A non-limiting example of Defendant's infringement is the Amazon Echo Show 10 (*e.g.*, model t4E4AT) which includes a Western Digital 15nm 64G 2D NAND Memory chip which infringes at least claim 1 of the '701 patent. Exemplary photographs of the Amazon Echo Show 10 are set forth below:



122. The various components of the Amazon Echo Show 10, including a SanDisk memory chip, are shown below:

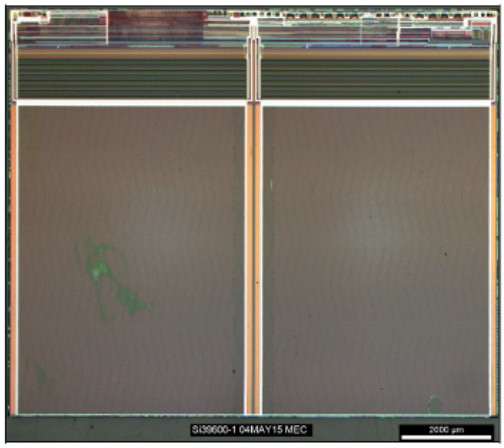


123. The components of the SanDisk memory chip, including the SanDisk FKB7 NAND Flash memory chip are shown below:



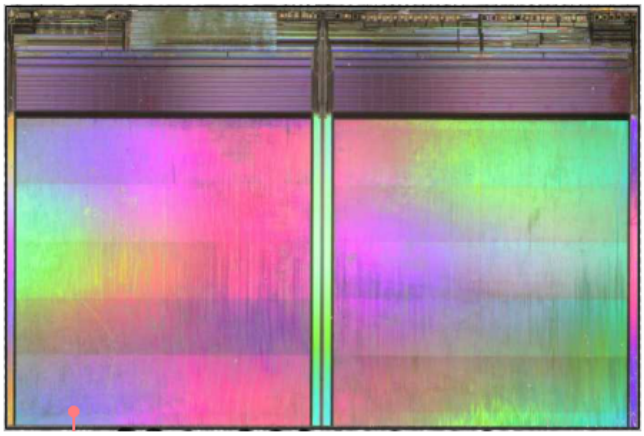
124. On information and belief, the SanDisk FKB7 NAND Flash memory chip is substantially similar to the Toshiba FFK8 NAND Flash memory chip

("Toshiba FFK8") for all matters relevant to this complaint. The Toshiba FFK8 is depicted below. A side-by-side comparison of the SanDisk FKB7 NAND Flash memory and the Toshiba FFK8 NAND Flash memory chip is depicted below:



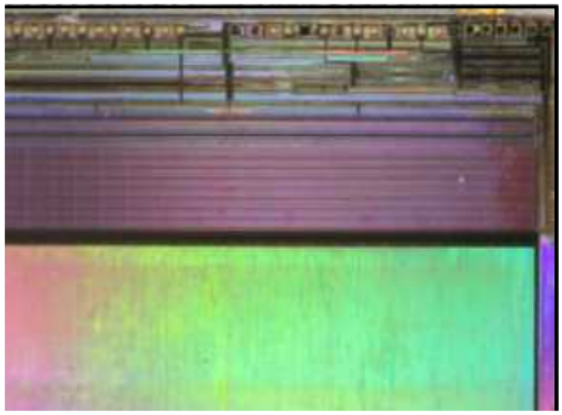
Photograph 2.2.1: Die photograph

FFK8 128G



FKB7

FFK8 128G



FKB7

125. Based at least on the above, Longitude is informed and believes that the corners of the dies of the SanDisk FKB7 NAND Flash memory and the Toshiba FFK8 NAND Flash memory chip are substantially the same. Accordingly, Longitude is informed and believes that the various I/Os and peripheral circuits are the same between the two chips. Furthermore, Longitude is informed and believes that Toshiba and Western Digital shared the designs for the chips. As shown above,

the SanDisk memory chip is substantially the same as the SanDisk FKB7 NAND Flash memory and the Toshiba FFK8 NAND Flash memory chip. For this reason, Longitude is informed and believes that technical documents and other analysis concerning the Toshiba FFK8 NAND Flash memory chip also describe the layout and functionality of the SanDisk FKB7 NAND Flash memory.

126. The SanDisk FKB7 NAND Flash memory within the Amazon Echo Show 10 performs a method for generating a voltage supply:

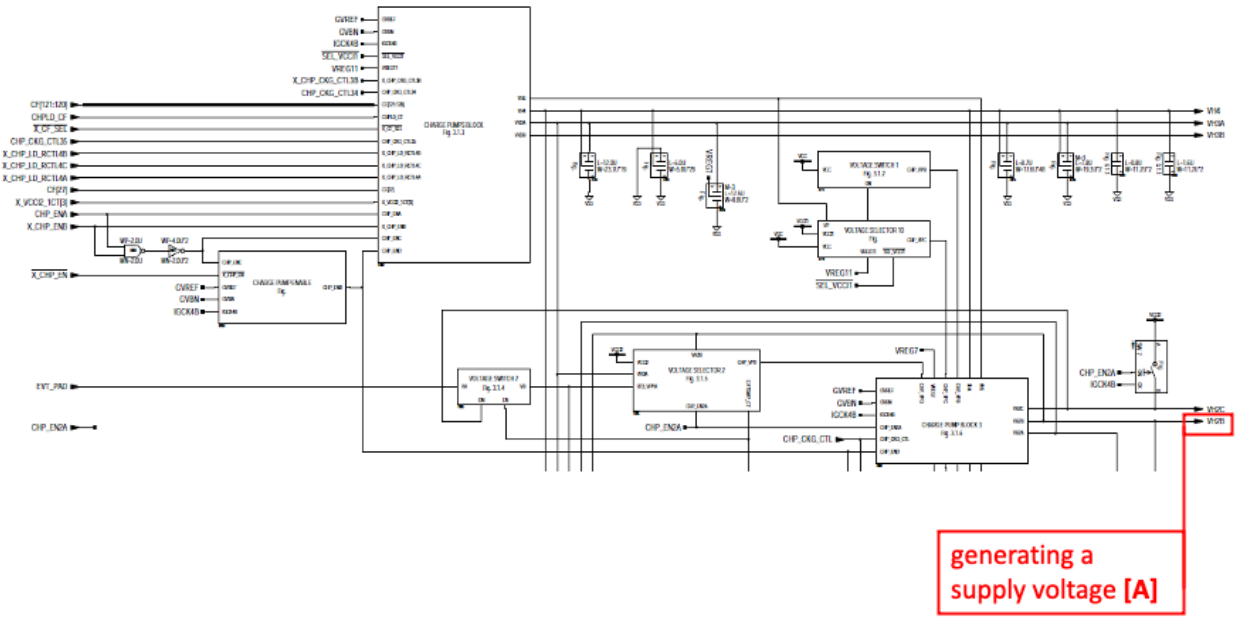


Figure 3.1 CHARGE PUMP SYSTEM

127. The SanDisk FKB7 NAND Flash memory within the Amazon Echo Show 10 performs a method of generating a voltage supply, comprising one of a first input node supplied with a first power supply voltage and a second input node supplied with a second power supply voltage that is higher than the first power supply voltage:

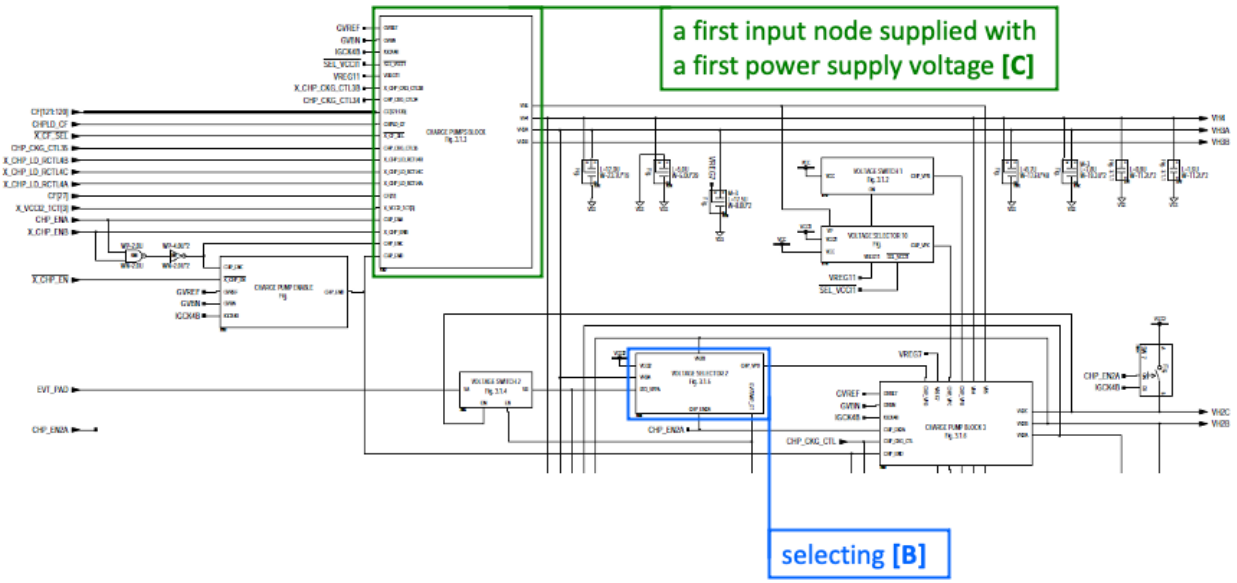


Figure 3.1 CHARGE PUMP SYSTEM

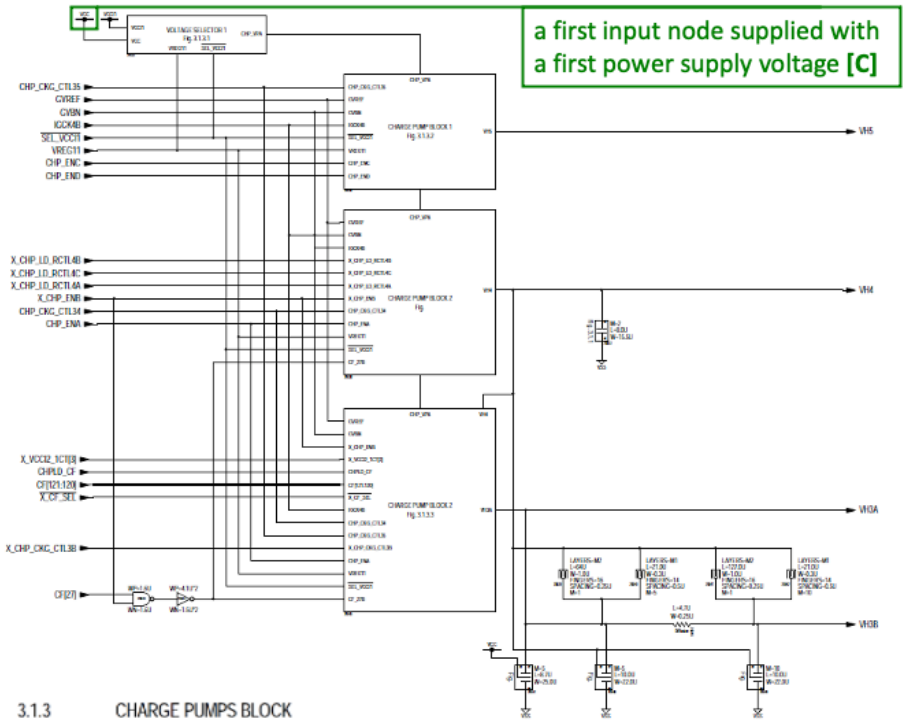


Figure 3.1.3 CHARGE PUMPS BLOCK

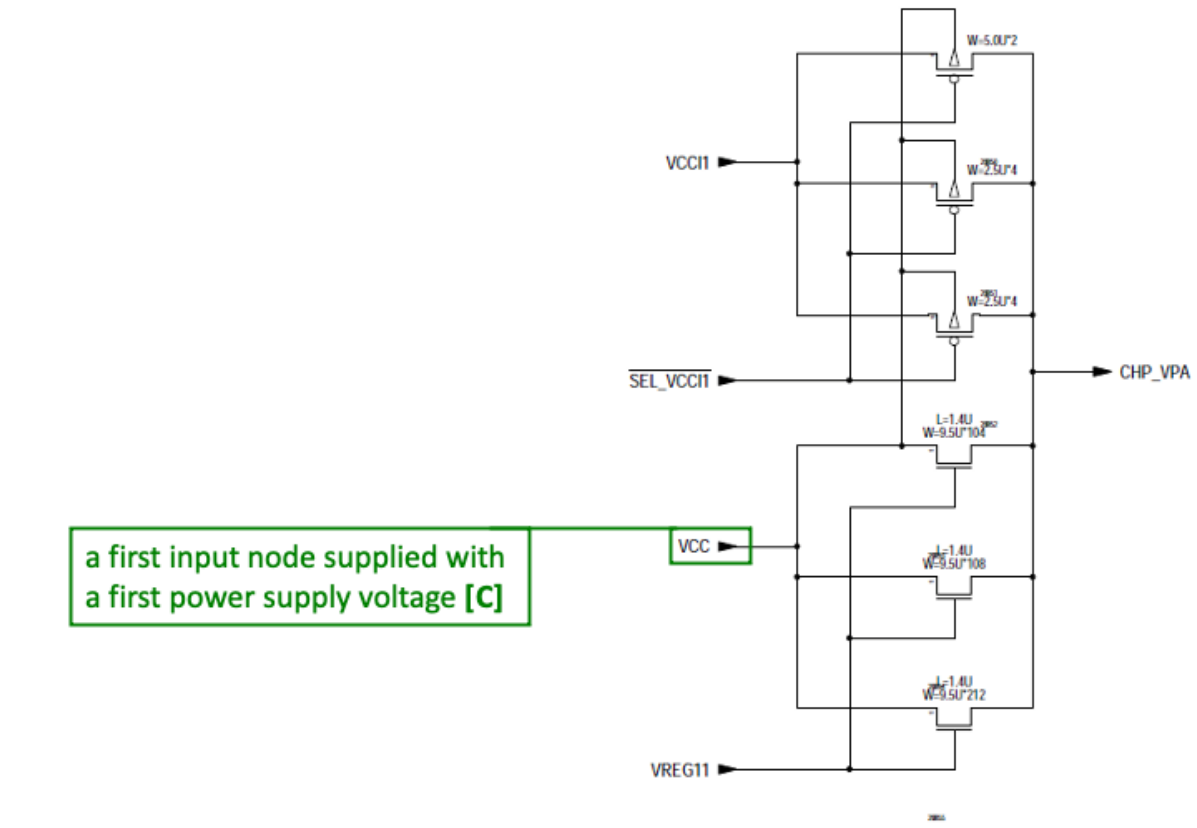


Figure 3.1.3.1 VOLTAGE SELECTOR 1

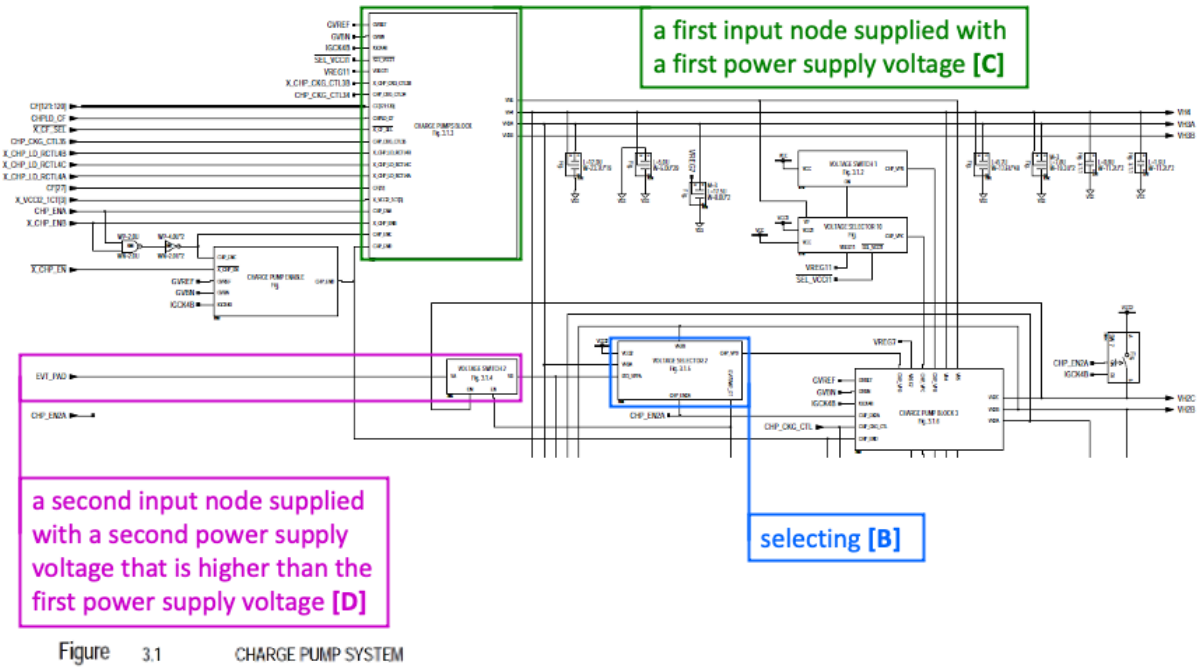


Figure 3.1 CHARGE PUMP SYSTEM

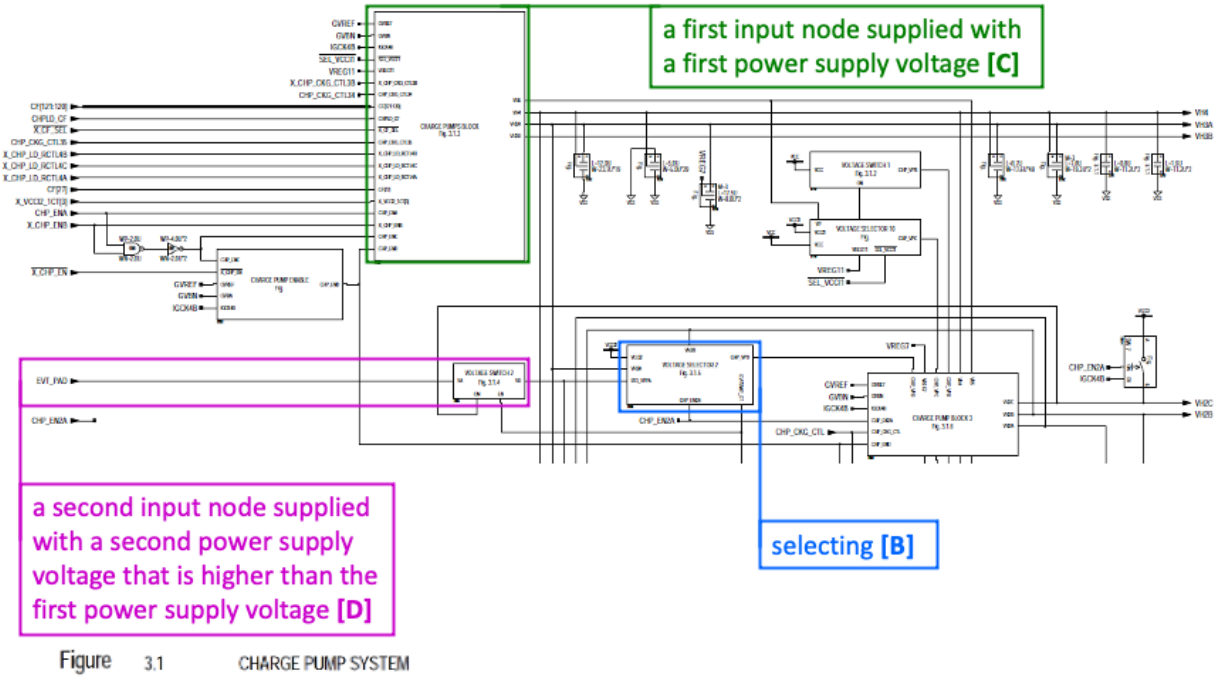


Figure 3.1 CHARGE PUMP SYSTEM

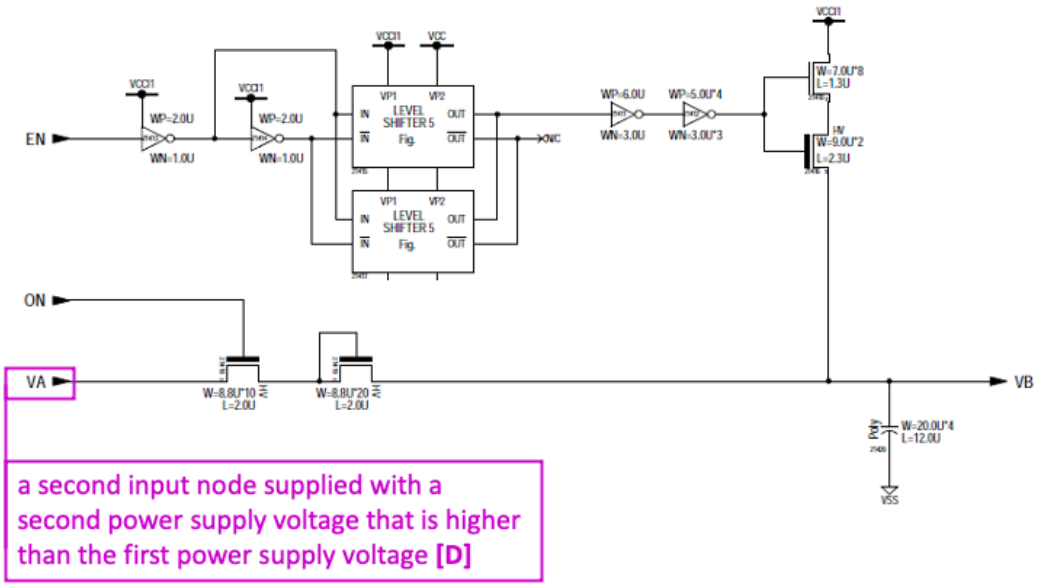


Figure 3.1.4 VOLTAGE SWITCH 2

128. The SanDisk FKB7 NAND Flash memory within the Amazon Echo Show 10 performs a method of generating a voltage supply, further comprising coupling a selected one of the first and second input nodes to booster circuitry

comprising a plurality of booster stages to provide an output voltage, wherein selection of the first input node corresponds to a first number of booster stages and selection of the second input node corresponds to selection of a second number of booster stages, the second number being less than the first number:

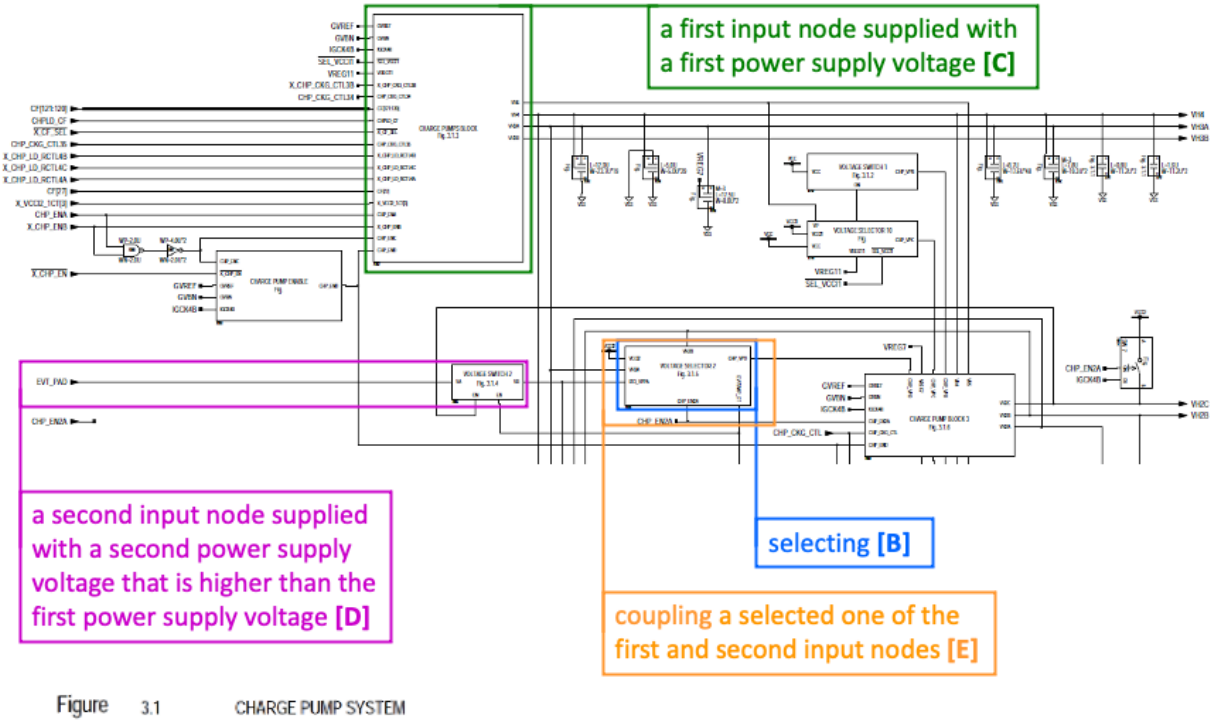


Figure 3.1 CHARGE PUMP SYSTEM

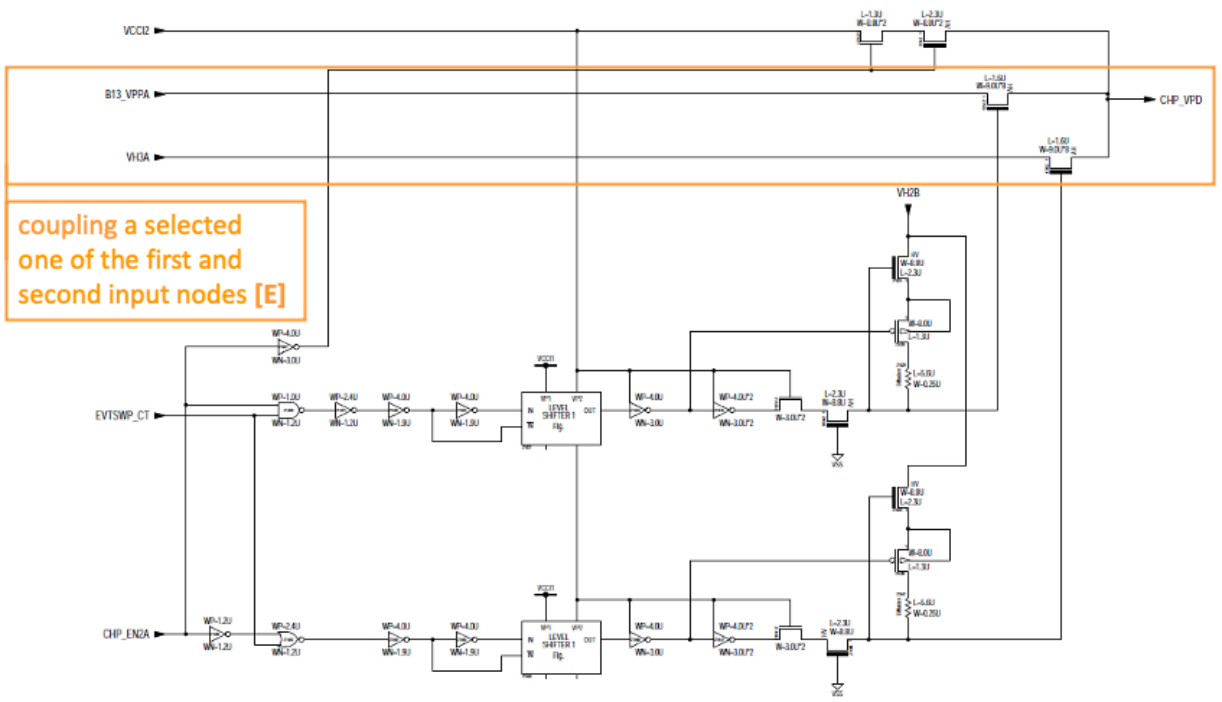


Figure 3.1.5 VOLTAGE SELECTOR 2

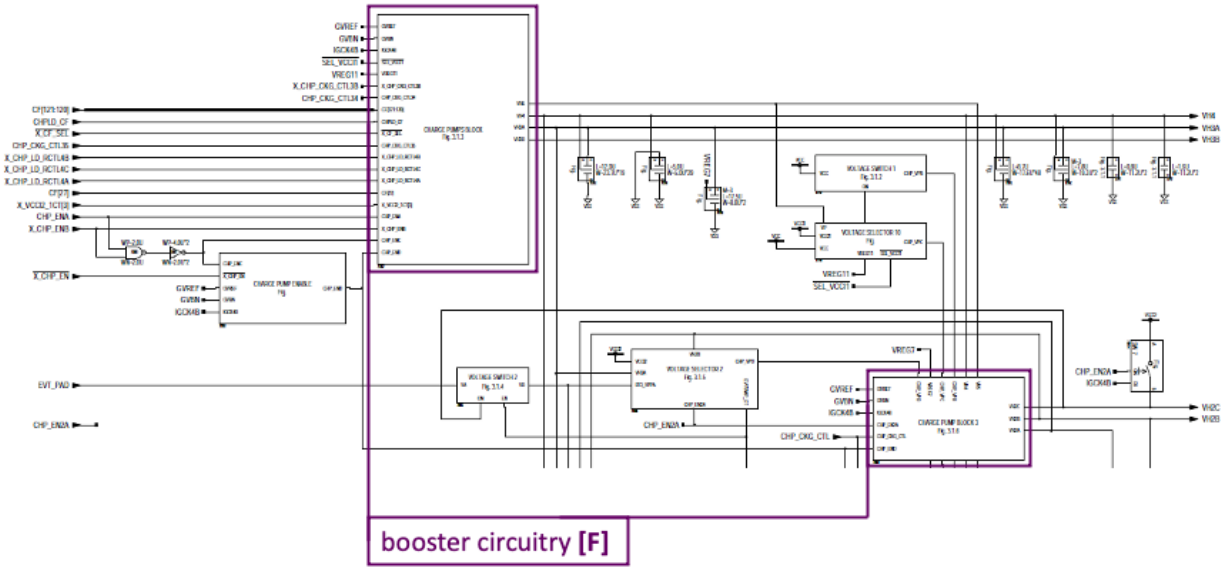


Figure 3.1 CHARGE PUMP SYSTEM

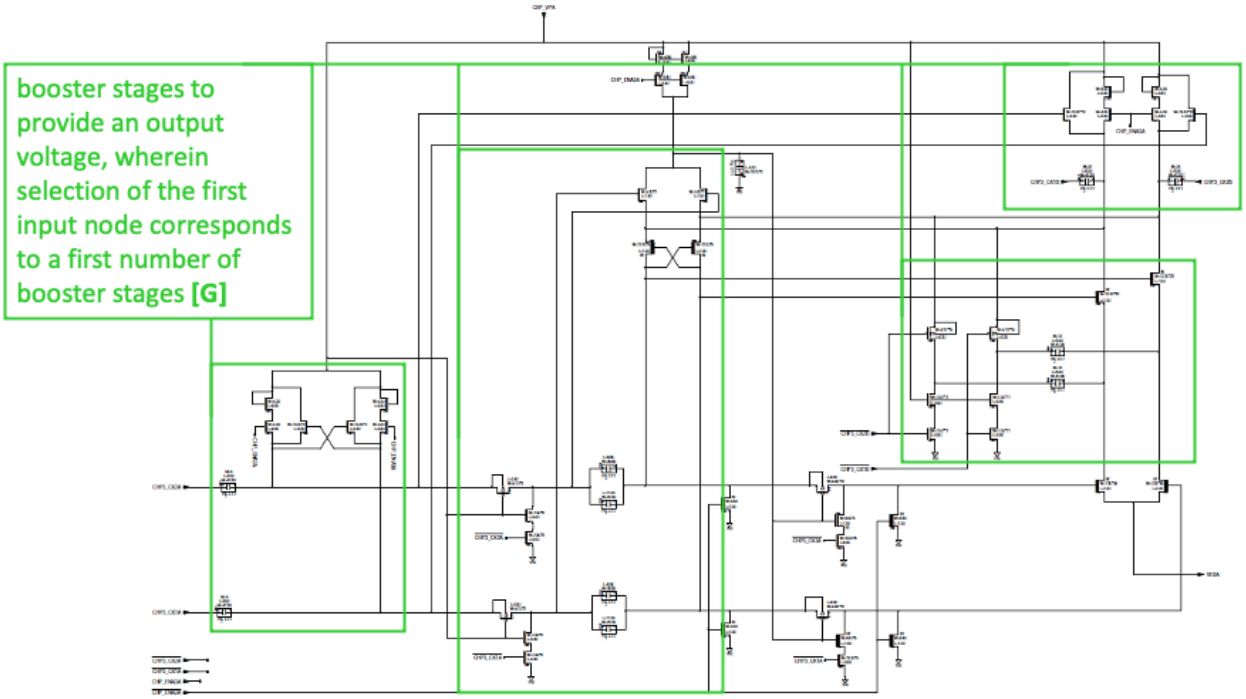


Figure 3.1.3.3.1 CHARGE PUMP 2

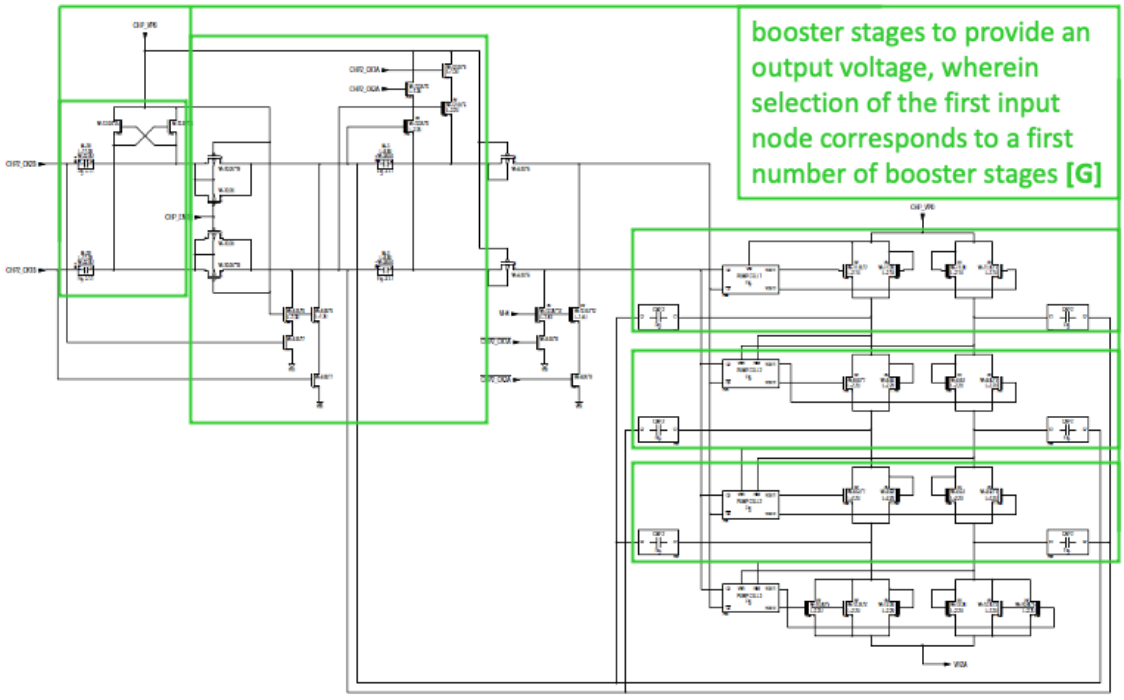


Figure 3.1.6.3 CHARGE PUMP 3

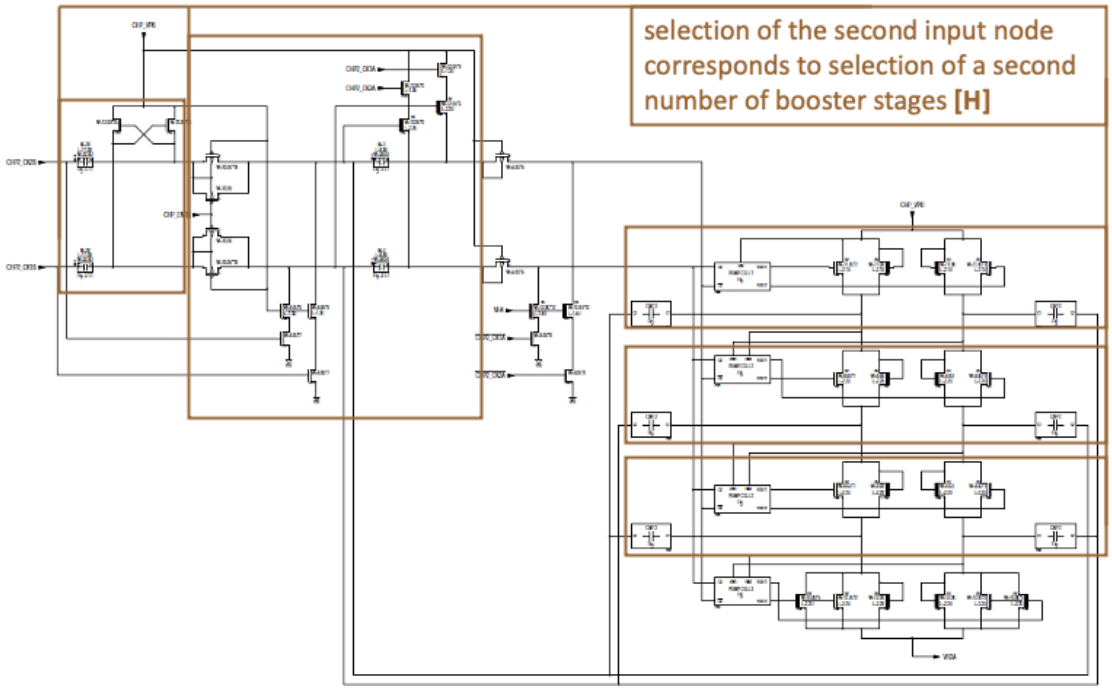


Figure 3.1.6.3 CHARGE PUMP 3

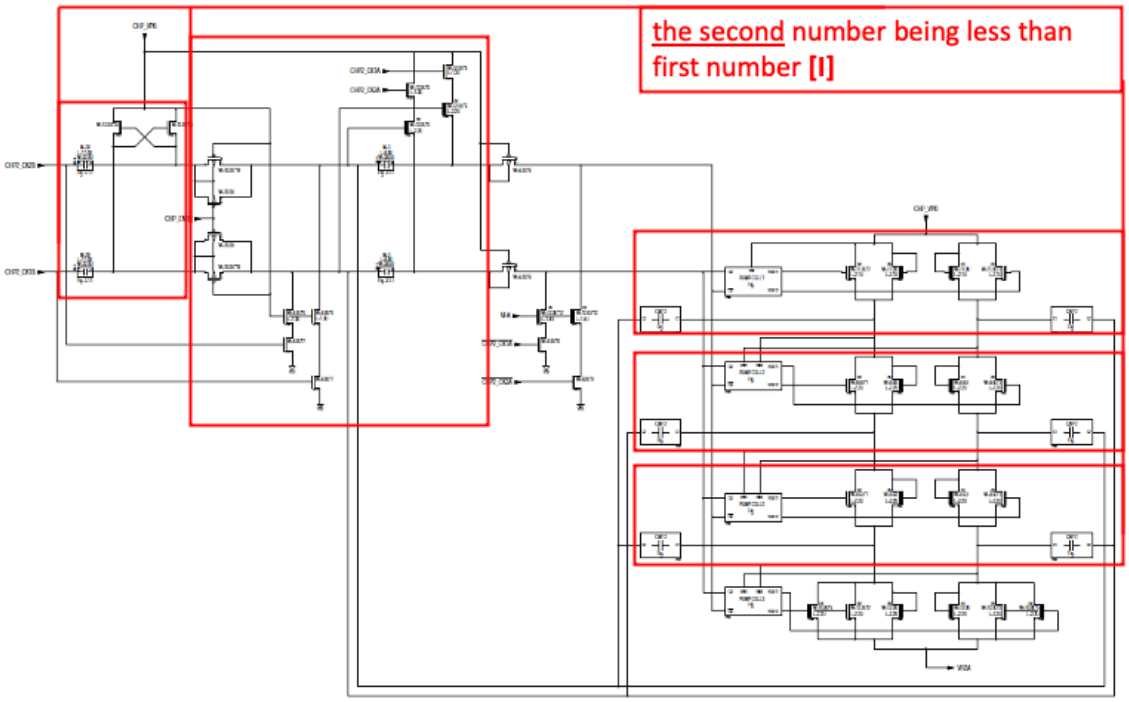


Figure 3.1.6.3 CHARGE PUMP 3

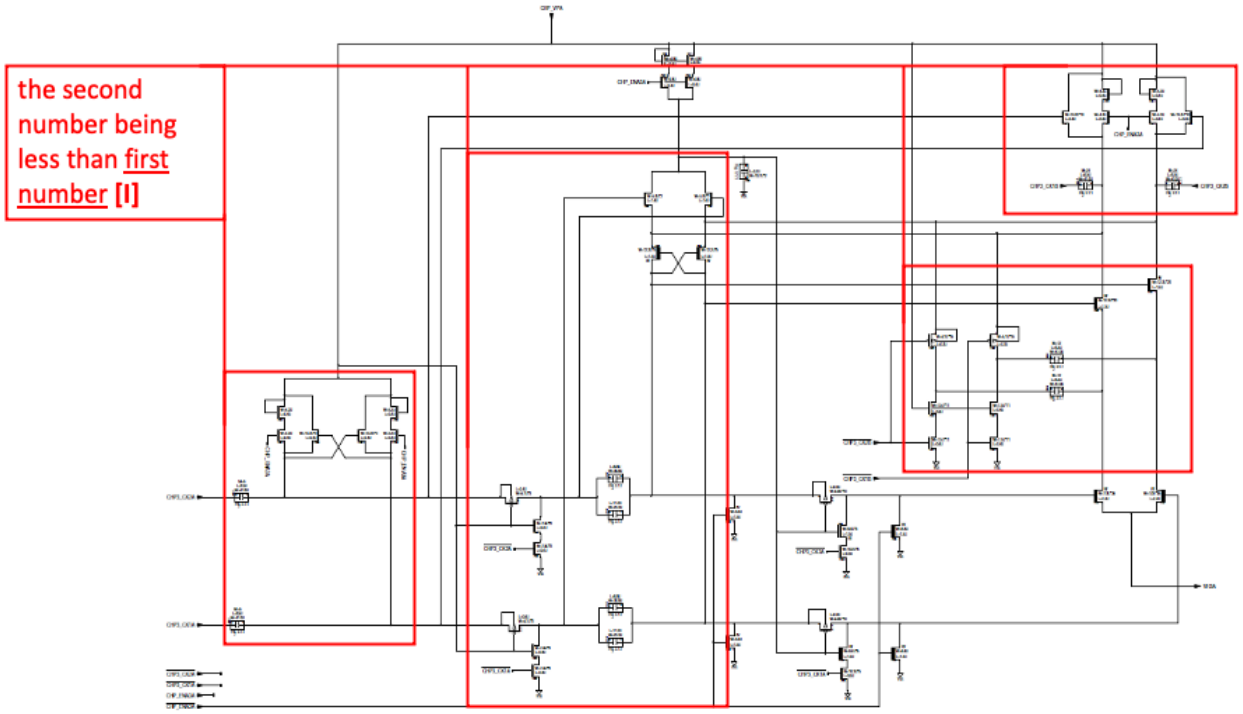


Figure 3.1.3.3.1 CHARGE PUMP 2

129. The SanDisk FKB7 NAND Flash memory within the Amazon Echo Show 10 performs a method of generating a voltage supply, further comprising changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected:

changing the booster circuitry from the first number of booster stages corresponding to selection of the first input node to the second number of booster stages when the second input node is selected **[J]**

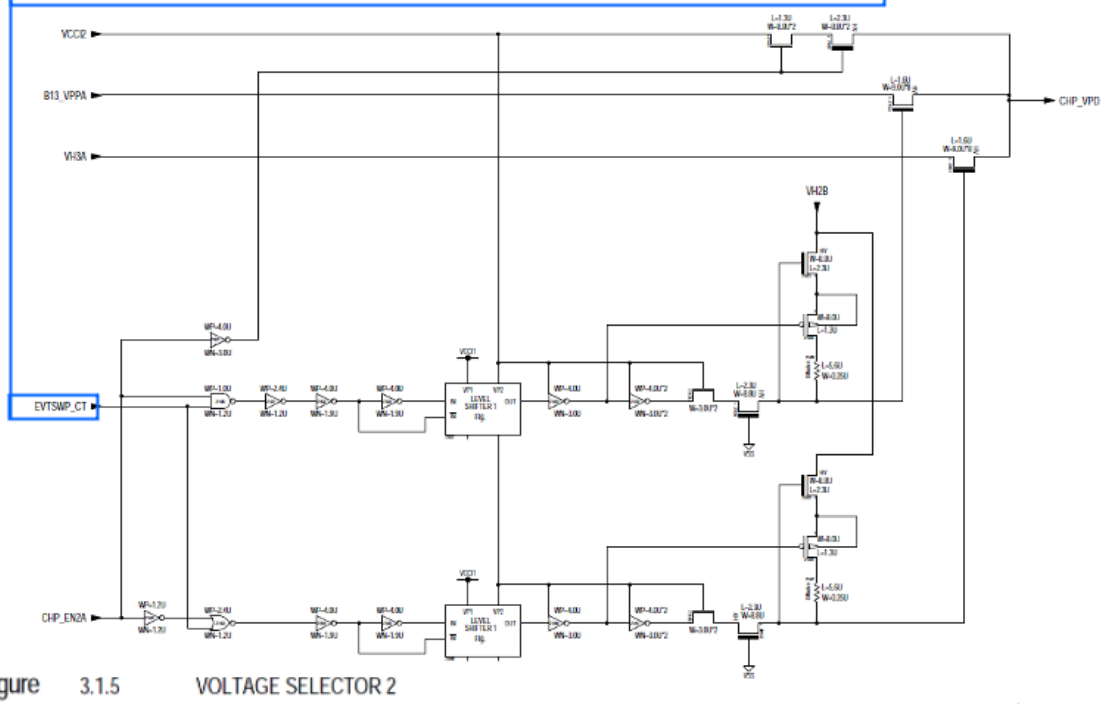


Figure 3.1.5 VOLTAGE SELECTOR 2

130. Defendant actively, knowingly, and intentionally induces, and continues to actively, knowingly, and intentionally induce, infringement of the '701 patent under 35 U.S.C. §271(b) by its customers and end users.

131. Defendant has had knowledge of and notice of the '701 patent and its infringement since at least September 6, 2022 when Longitude gave Defendant notice of its infringing actions. In any event, Defendant has had knowledge and notice of the '701 patent since at least the filing of this complaint.

132. Defendant has induced its customers and end users to infringe the '701 patent by using their products as shown above. For example, Defendant encourages its customers and end users to perform infringing methods by the very nature of the products.

133. Defendant specifically intends that its customers and/or end users infringe the '701 patent, either literally or by the doctrine of equivalents, because Defendant has known about the '701 patent and how Defendant's products infringe the claims of the '701 patent but Defendant has not taken steps to prevent

infringement by its customers and/or end users. Accordingly, Defendant has acted with the specific intent to induce infringement of the '701 patent.

134. Accordingly, Defendant has induced, and continues to induce, infringement of the '701 patent under 35 U.S.C. §271(b).

135. As discussed above, Defendant has had knowledge of and notice of the '701 patent and its infringement since at least September 6, 2022. Despite this knowledge, Defendant continues to commit tortious conduct by way of patent infringement.

136. Defendant has been and continues to infringe one or more of the claims of the '701 patent through the aforesaid acts.

137. Defendant has committed these acts of infringement without license or authorization.

138. Plaintiff is entitled to recover damages adequate to compensate for the infringement.

139. Defendant has and continues to infringe the '701 patent, acting with an objectively high likelihood that its actions constitute infringement of the '701 patent. Defendant has known or should have known of this risk at least as early as September 6, 2022. Accordingly, Defendant's infringement of the '701 patent has been and continues to be willful.

PRAYER FOR RELIEF

Wherefore, Longitude, respectfully requests the following relief:

a) A judgment that Defendant has infringed the '369 patent;

b) A judgment that Defendant has infringed the '539 patent;

c) A judgement that Defendant has infringed the '233 patent;

d) A judgement that Defendant has infringed the '701 patent;

e) A judgment that awards Plaintiff all appropriate damages under 35 U.S.C. § 284 for Defendant's past infringement, and any continuing or future infringement of the Patents-in-Suit, up until the date such judgment is entered,

including interest, costs, and disbursements as justified under 35 U.S.C. § 284 to adequately compensate Plaintiff for Defendant's infringement;

f) An adjudication that Defendant's infringement of the Patents-in-Suit has been willful and deliberate;

g) An adjudication that Plaintiff be awarded treble damages and pre-judgment interest under 35 U.S.C. § 284 as a result of Defendant's willful and deliberate infringement of the Patents-in-Suit;

h) An adjudication that this case is exceptional within the meaning of 35 U.S.C. § 285;

i) An adjudication that Plaintiff be awarded the attorneys' fees, costs, and expenses it incurs in prosecuting this action; and

j) An adjudication that Plaintiff be awarded such further relief at law or in equity as the Court deems just and proper.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Respectfully submitted,

DATED: January 9, 2023

RUSS, AUGUST & KABAT

/s/ Brian D. Ledahl

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